Zmluva
o poskytnutí finančných prostriedkov na spolufinancovanie
projektu výskumu a vývoja ENIAC č. 324280/2012
Časť projektu: „Multipulzné testovanie spoľahlivosti výkonových prvkov pomocou UIS testovania pri vysokých teplotách“

Poskytovateľ:	**Ministerstvo školstva, vedy, výskumu a športu SR**
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zastúpený štatutárnym. orgánom:	doc. PhDr. Dušanom Čaplovičom, DrSc. ministrom
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(ďalej len „poskytovateľ“)

Príjemca:	**NanoDesign, s.r.o.**
sídlo:	Drotárska 6385/19a, 811 04, Bratislava
zastúpený štatutárnym orgánom:	Ing. Martin Daříček, PhD.
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(ďalej len „príjemca “)

Preambula

Nariadením Rady (ES) č. 72/2008 z 20. decembra 2007 bol založený spoločný európsky technologický podnik ENIAC (ďalej len „spoločný podnik“) na podporu spoločných európskych výskumných a vývojových aktivít v oblasti nanoelektroniky. Slovenská republika sa prihlásila za člena spoločného podniku listom podpredsedu vlády a ministra školstva SR zo dňa 12. decembra 2008 a zaviazala sa alokovať každoročne v rozpočtovej kapitole Ministerstva školstva Slovenskej republiky prostriedky štátneho rozpočtu Slovenskej republiky vo výške 500 000 eur za účelom spolufinancovania účasti organizácií výskumu a vývoja v Slovenskej republike v projektoch výskumu a vývoja spoločného podniku (ďalej len „projekt spoločného podniku“).

Na základe dohody o administrácii č. ENIAC-ED-27-09 uzavretej medzi spoločným podnikom a Ministerstvom školstva SR, ktorá je neoddeliteľnou súčasťou tejto zmluvy v Prílohe 1, sa Ministerstvo školstva SR stalo národným financujúcim orgánom, ktorý zabezpečuje poskytovanie prostriedkov štátneho rozpočtu Slovenskej republiky na spolufinancovanie účasti organizácií výskumu a vývoja v Slovenskej republike v projektoch spoločného podniku.

Čl. 1
Predmet zmluvy

1) Poskytovateľ a príjemca uzatvárajú túto zmluvu podľa Čl. 13 ods. 6 písm. b) Štatútu spoločného podniku ENIAC, ktorý je neoddeliteľnou súčasťou Nariadenia Rady (ES) č. 72/2008 z 20. decembra 2007, ktorým sa zakladá spoločný podnik ENIAC (ďalej len „štatút spoločného podniku“).

2) Poskytovateľ a príjemca sa dohodli na predmete zmluvy na základe technickej špecifikácie Technical Anex E2COGaN – Energy Efficient Converters using GaN Power Devices (ďalej len „technická špecifikácia), ktorá bola schválená spoločným podnikom dňa 9. januára 2013 a je v Prílohe 2 k tejto zmluve, ktorá je jej neoddeliteľnou súčasťou.

3) Predmetom zmluvy je poskytnutie 94 500 EUR (slovom deväťdesiatštyritisíc päťsto EUR) z prostriedkov štátneho rozpočtu Slovenskej republiky poskytovateľom príjemcovi na zabezpečenie spolufinancovania riešenia projektu spoločného podniku s názvom “Energeticky efektívne konvertory na báze GaN výkonových súčiastok (E2COGaN)“, ktorého riešenie bolo schválené na základe výberového konania uskutočneného spoločným podnikom k výzve ENIAC Call 2012-1 pre verejnú súťaž ním vyhlásenej v roku 2012 a potvrdené „technickou špecifikáciou“.

4) Doba riešenia projektu spoločného podniku je stanovená v „technickej špecifikácií“ schválenej spoločným podnikom.

5) Poskytovateľ zabezpečuje spolufinancovanie riešenia projektu spoločného podniku počas celej doby jeho riešenia, ktorá je 36 mesiacov.

6) Príjemca sa zaväzuje zabezpečiť riešenie projektu č. 324280/2012 s názvom: “Energeticky efektívne konvertory na báze GaN výkonových súčiastok“, (“E2COGaN – Energy Efficient Converters using GaN Power Devices“), časť projektu: „Multipulzné testovanie spoľahlivosti výkonových prvkov pomocou UIS testovania pri vysokých teplotách“ počas celej doby jeho riešenia od: 01/04/2013 do: 31/03/2016.

7) Špecifikácia projektu spoločného podniku (zoznam riešiteľov a ich kapacít viazaných na riešenie projektu, použitia prostriedkov štátneho rozpočtu Slovenskej republiky poskytnutých poskytovateľom vrátane charakteristiky, cieľov projektu v jednotlivých rokoch jeho riešenia a výstupov) je uvedená v Prílohe 3, ktorá je neoddeliteľnou súčasťou zmluvy.

Čl. 2
Poskytovanie a použitie prostriedkov

1) Financovanie projektu spoločného podniku sa uskutočňuje podľa Čl. 13 štatútu spoločného podniku.

2) Spoločný podnik podľa Čl. 13 ods. 6 písm. a) štatútu spoločného podniku poskytuje príjemcovi na spolufinancovanie riešenia projektu spoločného podniku prostriedky zo svojho rozpočtu vo výške 15,0 % z celkových oprávnených nákladov na riešenie projektu spoločného podniku.

3) Poskytovateľ poskytuje príjemcovi, ktorý je podnikateľom podľa zákona č. 513/1991 Zb. (Obchodný zákonník) v znení neskorších predpisov na spolufinancovanie riešenia projektu spoločného podniku prostriedky štátneho rozpočtu Slovenskej republiky vo výške 35,0 % z celkových oprávnených nákladov na riešenie projektu spoločného podniku.

4) Oprávnenými nákladmi na riešenie projektu spoločného podniku, ktoré financuje poskytovateľ z prostriedkov štátneho rozpočtu Slovenskej republiky, sú náklady podľa § 17 ods. 2 až 5 zákona č. 172/2005 Z. z. o organizácii štátnej podpory výskumu a vývoja a o doplnení zákona č. 575/2001 Z. z. o organizácii činnosti vlády a organizácii ústrednej štátnej správy v znení neskorších predpisov v znení neskorších predpisov a rozpočet projektu spoločného podniku hradený z prostriedkov štátneho rozpočtu Slovenskej republiky je špecifikovaný príjemcom v časti C. Prílohy 3 k tejto zmluve.

5) Príjemca si za účelom poskytnutia prostriedkov štátneho rozpočtu Slovenskej republiky poskytovateľom a ich transparentného čerpania zriadi osobitný účet (ďalej len „účet príjemcu“).

6) Poskytovateľ poskytuje prostriedky štátneho rozpočtu Slovenskej republiky na účet príjemcu v jednotlivých rokoch riešenia projektu spoločného podniku podľa rozpisu celkových oprávnených nákladov uvedených v Prílohe 4 k tejto zmluve, ktorá je jej neoddeliteľnou súčasťou.

7) V prvom rozpočtovom roku riešenia projektu poskytovateľ poskytne prostriedky štátneho rozpočtu Slovenskej republiky na účet príjemcu v lehote do 20 pracovných dní odo dňa účinnosti tejto zmluvy.

8) V ďalších rokoch riešenia projektu spoločného podniku poskytovateľ poskytuje prostriedky štátneho rozpočtu Slovenskej republiky na účet príjemcu na základe výsledkov monitorovania a technického auditu projektu spoločného podniku, ktoré vykonáva spoločný podnik a na základe kontroly použitia prostriedkov štátneho rozpočtu Slovenskej republiky poskytnutých príjemcovi v predchádzajúcom rozpočtovom roku, ktorú vykonáva poskytovateľ.

9) Poskytovateľ poskytuje prostriedky štátneho rozpočtu Slovenskej republiky v ďalších rokoch riešenia projektu spoločného podniku na účet príjemcu na základe dodatkov k tejto zmluve.

10) Ak v prvom rozpočtovom roku riešenia projektu spoločného podniku sú prostriedky štátneho rozpočtu Slovenskej republiky poskytnuté poskytovateľom omeškane na účet príjemcu voči termínu začatia riešenia projektu spoločného podniku, ktorý je záväzne stanovený spoločným podnikom v „technickej špecifikácii“, z dôvodu omeškania podpísania zmluvy medzi príjemcom a poskytovateľom alebo medzi príjemcom a spoločným podnikom, môže príjemca na financovanie projektu spoločného podniku použiť vlastné prostriedky, ktoré si potom refunduje z prostriedkov vedených na účte príjemcu.

11) Rovnako v ďalších rokoch riešenia projektu spoločného podniku, ak poskytovateľ poskytne prostriedky štátneho rozpočtu Slovenskej republiky na účet príjemcu omeškane, môže príjemca počas meškania použiť na riešenie projektu spoločného podniku vlastné prostriedky, ktoré si potom refunduje z prostriedkov vedených na účte príjemcu.

12) Príjemca môže prostriedky štátneho rozpočtu Slovenskej republiky poskytnuté poskytovateľom na účet príjemcu použiť iba na stanovený účel.

13) Bežné výdavky, ktoré boli poskytnuté príjemcovi po 1. októbri rozpočtového roka, a ktoré nebolo možné použiť do konca príslušného rozpočtového roka možno použiť do 31. marca nasledujúceho rozpočtového roka v súlade s § 8 ods. 5 zákona č. 523/2004 Z. z. o rozpočtových pravidlách verejnej správy a o zmene a doplnení niektorých zákonov.

14) Použitie finančnej dotácie podlieha povinnému ročnému zúčtovaniu so štátnym rozpočtom v zmysle § 8a ods. 7 zákona č. 523/2004 Z. z. o rozpočtových pravidlách verejnej správy a o zmene a doplnení niektorých zákonov najneskôr v termíne a spôsobom určenom Ministerstvom financií SR na zúčtovanie finančných prostriedkov štátneho rozpočtu. Zúčtovanie finančnej dotácie poskytnutej prijímateľovi v nasledujúcich kalendárnych rokoch v zmysle dodatkov k tejto zmluve bude vykonané v zmysle podmienok stanovených Ministerstvom financií SR k zúčtovaniu finančných vzťahov so štátnym rozpočtom na daný kalendárny rok.

15) Prostriedky vyplývajúce zo zúčtovania je príjemca povinný bez zbytočného odkladu vrátiť po 31. 3. 2013 na depozitný účet poskytovateľa 7000063900/8180, Štátna pokladnica, variabilný symbol číslo 11. O vratke nepoužitých prostriedkov je príjemca povinný poslať písomné oznámenie odboru učtárne a styku so Štátnou pokladnicou poskytovateľa.

16) Príjemca zodpovedá za hospodárenie s prostriedkami štátneho rozpočtu Slovenskej republiky poskytnutými poskytovateľom na účet príjemcu a je povinný pri ich použití zachovávať hospodárnosť, efektívnosť a účelnosť ich použitia.

17) Výnos, ktorý vznikol z účtu príjemcu, je podľa § 7 ods. 1 písm. m) zákona č. 523/2004 Z. z. o rozpočtových pravidlách verejnej správy a o zmene a doplnení niektorých zákonov v znení neskorších predpisov v spojení s Metodickým usmernením Ministerstva financií Slovenskej republiky číslo MF/7415/2005-421 príjmom štátneho rozpočtu Slovenskej republiky.

18) Výnosom určeným na vykonanie odvodu, sú prostriedky, ktoré zostali na účte príjemcu po odpočítaní celého poplatku za vedenie účtu príjemcu od úrokov pripisovaných bankou.

19) Lehota na vykonanie odvodu výnosov z prostriedkov štátneho rozpočtu Slovenskej republiky vedených na účte príjemcu na účet poskytovateľa č. 7000063812/8180 je do 31.3. nasledujúceho rozpočtového roka.

20) Ak riešenie projektu spoločného podniku vyžaduje zaobstaranie tovarov, služieb a prác, príjemca je povinný v cene pre ich zaobstaranie zohľadniť najlepší pomer kvality a výšky ceny.

21) Príjemca pri zaobstarávaní tovarov, služieb a prác z prostriedkov štátneho rozpočtu Slovenskej republiky vedených na účte príjemcu musí postupovať podľa zákona č. 25/2006 Z. z. o verejnom obstarávaní a o zmene a doplnení niektorých zákonov v znení neskorších predpisov.

Čl. 3
Práva a povinnosti

1) Príjemca a poskytovateľ zodpovedajú za včasné a riadne plnenie si povinností podľa tejto zmluvy.

2) Príjemca je povinný všetky náklady súvisiace s riešením projektu doložiť prehľadom o výške, spôsobe a účele čerpania finančných prostriedkov, vypracovaných podľa skutočných nákladov na riešenie projektu a platných usmernení a pokynov poskytovateľa v termíne do 31. januára nasledujúceho rozpočtového roka.

3) Príjemca je povinný uchovávať všetky dokumenty a doklady, vrátane účtovných dokladov, týkajúcich sa projektu spoločného podniku najmenej počas piatich rokov nasledujúcich po roku, kedy skončí doba spolufinancovania projektu spoločného podniku poskytovateľom.

Čl. 4
Kontrola

1) Monitorovanie a kontrolu riešenia projektu spoločného podniku vykonáva spoločný podnik podľa Čl. 7 ods. 3 písm. j) a k) štatútu spoločného podniku.

2) Poskytovateľ akceptuje závery vyplývajúce z monitorovacích správ a výsledkov kontroly riešenia projektu spoločného podniku vykonaných spoločným podnikom.
3) Poskytovateľ je oprávnený vykonať pre svoje potreby finančnú kontrolu podľa zákona č. 502/2001 Z. z. o finančnej kontrole a vnútornom audite a o zmene a doplnení niektorých zákonov v znení neskorších predpisov počas trvania zmluvného vzťahu medzi ním a príjemcom ako aj po jeho ukončení, a to aj v prípade odstúpenia od zmluvy.

4) Príjemca je povinný pri výkone kontroly alebo auditu dodržiavať ustanovenia § 14 ods. 2 a § 35 ods. 8 zákona č. 502/2001 Z. z. o finančnej kontrole a vnútornom audite a o zmene a doplnení niektorých zákonov v znení neskorších predpisov.

Čl. 5
Odstúpenie od zmluvy

1) Poskytovateľ má právo odstúpiť od zmluvy, ak
   a) si príjemca neplní povinnosti stanovené v tejto zmluve,
   b) riešenie projektu spoločného podniku má závažné chyby, ktoré zistil spoločný podnik pri monitorovaní a kontrole riešenia projektu spoločného podniku, alebo také chyby, že čas na ich odstránenie by do značnej miery znehodnotil cieľ riešenia projektu spoločného podniku,
   c) spoločný podnik odstúpi od zmluvy medzi ním a príjemcom z ďalších dôvodov stanovených v zmluve medzi ním a príjemcom,
   d) dôjde k zrušeniu spoločného podniku.

2) Ak poskytovateľ odstúpi od zmluvy medzi ním a príjemcom z dôvodov podľa Čl. 5 ods. 1 písm. a) až c) tejto zmluvy, má právo požadovať vrátenie všetkých prostriedkov štátneho rozpočtu Slovenskej republiky ním poskytnutých príjemcovi.

3) Ak poskytovateľ odstúpi od zmluvy medzi ním a príjemcom z dôvodov podľa Čl. 5 ods. 1 písm. d), má právo požadovať vrátenie časti prostriedkov štátneho rozpočtu Slovenskej republiky, ktoré boli použité príjemcom po termíne zrušenia spoločného podniku.

4) Príjemca pri naplnení ods. 2 Čl. 5 a ods. 3 Čl. 5 zmluvy poskytnuté prostriedky vráti bez zbytočného odkladu a to:
   - na výdavkový účet poskytovateľa č. 7000065236/8180, ak sa prostriedky vracajú v tom istom rozpočtovom roku, v ktorom boli poskytnuté príjemcovi,
   - na príjmový účet poskytovateľa č. 7000063820/8180, ak sa prostriedky vracajú v inom rozpočtovom roku, v ktorom boli poskytnuté príjemcovi.

5) Príjemca má právo odstúpiť od zmluvy v prípade, ak si poskytovateľ neplní povinnosti stanovené v tejto zmluve.

6) Príjemca je povinný prostriedky štátneho rozpočtu Slovenskej republiky neoprávnene použité na iný účel než účel stanovený v predmete zmluvy vrátiť na príjmový účet poskytovateľa.

Čl. 6
Sankcie

Sankcie za porušenie finančnej disciplíny príjemcom pri hospodárení s prostriedkami štátneho rozpočtu Slovenskej republiky sa riadia § 31 zákona č. 523/2004 Z. z. o rozpočtových pravidlách verejnej správy a o zmene a doplnení niektorých zákonov v znení neskorších predpisov.

Čl. 7
Vlastnícke práva k predmetu zmluvy

Vlastnícke práva k výsledkom riešenia projektu spoločného podniku sa riadia podľa ustanovení Čl. 23 štatútu spoločného podniku.

Čl. 8
Záverečné ustanovenia

1) Príjemca a poskytovateľ sa zaväzujú bezodkladne navzájom sa písomne informovať o zmenách identifikačných údajov uvedených v zmluve a akýchkoľvek iných zmenách a skutočnostiach, ktoré by mohli mať vplyv na práva a povinnosti vyplývajúce z tejto zmluvy v lehote najneskôr do 30 kalendárnych dní.

2) Zmeny a doplnenia zmluvy môžu byť vykonané len prostredníctvom písomných dodatkov podpísaných obidvoma zmluvnými stranami.

3) Zmluva je vyhotovená v šiestich originálach, pričom každá zo zmluvných strán obdrží po tri exempláre.

4) Zmluva nadobúda platnosť dňom jej podpísania obidvoma zmluvnými stranami a účinnosť dňom nasledujúcom po jej zverejnení.

5) Prílohy k zmluve sú:
   a) Príloha 1: Dohoda o správe č. ENIAC-ED-27-09 uzavretá medzi spoločným podnikom a Ministerstvom školstva SR
   b) Príloha 2: Technická špecifikácia projektu – Technical Annex to E2COGaN – Energy Efficient Converters using GaN Power Devices
   c) Príloha 3: Špecifikácia projektu spoločného podniku
   d) Príloha 4: Rozpis celkových prostriedkov štátneho rozpočtu Slovenskej republiky na financovanie oprávnených nákladov projektu spoločného podniku v jednotlivých rokoch jeho riešenia
   e) Príloha 5: Predpokladaný rozpis celkových vlastných prostriedkov spolufinancovania NanoDesign, s.r.o. v projekte E2COGaN č. 324280/2012 spoločného podniku v jednotlivých rozpočtových rokoch jeho riešenia (v EUR).

V Bratislave dňa .....

V Bratislave dňa .....

.....
doc. PhDr. Dušan Čaplovič, DrSc.
minister

.....
Ing. Martin Daříček, PhD.
štatutárny orgán

Príloha č.1 k zmluve

Eniac JOINT UNDERTAKING

DOHODA O SPRÁVE MEDZI SPOLOČNÝM PODNIKOM ENIAC

A MINISTERSTVOM ŠKOLSTVA SLOVENSKEJ REPUBLIKY

1. Zmluvné strany

Tento materiál ustanovuje dohodu medzi spoločným podnikom ENIAC (ďalej len „Spoločný podnik“) a Ministerstvom školstva Slovenskej republiky (ďalej len „Národný financujúci orgán“), ktoré ustanovila Slovenská republika v súlade s čl.3 ods. 4 a čl. 12 a ods. 3 štatútu Spoločného podniku, ktorý je prílohou Nariadenia rady (EK) č. 72/2008 z 20. decembra 2007, a ktorým sa zakladá „Spoločný podnik ENIAC[1]“. Dohodou sa stanovujú vzťahy medzi Spoločným podnikom a národnými financujúcimi orgánmi určenými členskými štátmi ENIAC pre administratívne zabezpečenie implementácie projektov a poskytovanie verejných prostriedkov.

2. Rozsah

Táto dohoda detailne stanovuje požiadavky kladené na obidve straty za účelom implementácie projektov vybraných Spoločným podnikom. Je potrebné ju vykonávať v súlade s Nariadením rady (EK) č. 72/2008, ktorým sa zakladá „Spoločný podnik ENIAC“, výzvami Spoločného podniku na predkladanie návrhov projektov, rozpočtovými pravidlami Spoločného podniku podľa potreby a s členstvom Slovenskej republiky v Spoločnom podniku.

Táto dohoda je záväzná pre Spoločný podnik a Národný financujúci orgán ustanovený Slovenskou republikou.

3. Výklad tejto dohody

Národná financujúci orgán je povinná zabezpečiť výklad požiadaviek vyplývajúcich z tejto dohody a konať tak, aby umožnila implementácia projektov a poskytnutie verejných prostriedkov tak, ako je to stanovené v článku 12 odsek 3 štatútu Spoločného podniku.

Na zamedzenie nečestnému konaniu a podvodom je potrebné riadiť sa podľa Nariadenia Rady (EK, Euratom) č. 2988/95 zo dňa 18. decembra 1995 o ochrane finančných záujmov Európskych spoločenstiev[2], Nariadenia Rady (EK, Euratom) č. 2185/96 zo dňa 11. novembra 1996 týkajúceho sa

[1] OJ L 30. 4.2.2008, str. 21

[2] Ú. v. EÚ L 312, 23.12.1995, str. 1

kontrol na mieste a previerok uskutočňovaných Komisiou za účelom ochrany finančných záujmov Európskych spoločenstiev proti podvodom a iným nečestným konaniam[3] a Nariadenia (EK) č. 1073/1999 Európskeho parlamentu a Rady týkajúceho sa prešetrovaní ukončených Európskym úradom pre boj proti podvodom[4].

Výrazy, ktoré sa použijú v tomto materiáli, majú rovnaký význam ako v Nariadení Rady (EK) č. 72/2008, ktorým sa zakladá „Spoločný podnik ENIAC“, vo výzvach Spoločného podniku na predkladanie návrhov projektov a v rozpočtových pravidlách Spoločného podniku.

4. Národné zmluvy o grantoch

a) **Komunikácia o oprávnenosti národných kritérií**

Národný financujúci orgán zabezpečí komunikáciu so Spoločným podnikom ohľadom oprávnenosti národných kritérií a iných zákonných a finančných požiadaviek platných pre každú výzvu na predkladanie návrhov projektov za účelom zostavenia národných zmlúv o grantoch s riešiteľmi projektu. Tieto kritériá a požiadavky budú predložené Spoločnému podniku ešte pred zverejnením výzvy na predloženie návrhov projektov Spoločnému podniku, a do 30 dní od požiadavky výkonného riaditeľa.

Odsúhlasené oprávnené národné kritéria budú v zmysle predchádzajúceho odseku začlenené do výzvy na predloženie návrhov projektov Spoločnému podniku.

Národný financujúci orgán uzatvorí zmluvy o grantoch s riešiteľmi projektov v súlade s vlastnými vnútroštátnymi predpismi s prihliadnutím na:

(a) iba kritériá oprávnenosti, ktoré boli uvedené vo výzve alebo vo všetkých ďalších aktualizáciách výzvy;

(b) iné zákonné a finančné požiadavky na zostavenie národných zmlúv o grantoch, ktoré stanovujú národné zákony a predpisy, a ktoré boli odkonzultované so Spoločným podnikom v uzávierke podľa predchádzajúceho odseku.

b. Výber návrhov projektov

Spoločný podnik je zodpovedný za hodnotenie a výber návrhov projektov a za pridelenie verejných prostriedkov riešiteľom projektu podľa na výzvy na predkladanie návrhov projektov Spoločného podniku.

Predložené návrhy projektov sú posudzované nezávislými odborníkmi.

Rada verejných orgánov schváli zoznam vybraných návrhov projektov, doplnený údajmi o verejných prostriedkoch (Spoločného podniku a/alebo národného financujúceho orgánu) ako aj odporúčaniami na ďalšiu fázu rokovaní. Výkonný riaditeľ Spoločného podniku oznámi jednotlivým žiadateľom a Národnému financujúcemu orgánu tieto výsledky spoločne s bodovým hodnotením, pripomienkami a prípadnými odporúčaniami na zmeny do 15 dní od uskutočnenia výberu.

[3] Ú. v. EÚ L 295, 15.11.1996, str. 2

[4] Ú. v. EÚ L 139, 31.05.1999, str. 1

Na základe tejto komunikácie a v zmysle zoznamu vybraných návrhov projektov, ktoré schválila Rada verejných orgánov, začne Spoločný podnik v zastúpení výkonným riaditeľom technické rokovania s cieľom schváliť „Technickú špecifikáciu projektu[5]“ v rámci limitov vyjednávacieho mandátu a finančných zdrojov na riešiteľa projektu podľa rozhodnutia Rady verejných orgánov.

- V prípade, že boli technické rokovania úspešne ukončené, výkonný riaditeľ predloží ich výsledky spoločne s kompletnou príslušnou dokumentáciou riadiacej rade a Národnému financujúcemu orgánu za účelom vypracovania národnej zmluvy o grante.

- V prípade zmien, ktoré nemôže mandát Rady verejných orgánov vopred predpokladať alebo v prípade neúspešných technických rokovaní, výkonný riaditeľ predloží na schválenie Rade verejných orgánov výsledky rokovaní spoločne zo žiadosťou o zmenu projektu. Rozhodnutie Rady verejných orgánov predloží výkonný riaditeľ riadiacej rade a Národnému financujúcemu orgánu spoločne s kompletnou príslušnou dokumentáciou, aby mohla byť vypracovaná národnej zmluva o grante.

Po ukončení rokovaní predloží Spoločný podnik koordinátorovi zvoleného konzorcia na podpis zmluvu o grante Spoločného podniku a prístupové podklady.

c) Vypracovanie národných zmlúv o grantoch

Po ukončení výberového konania a rokovania, ktoré uskutočnil Spoločný podnik, Národný financujúci orgán vypracuje spoločne s riešiteľmi projektov národné zmluvy o grantoch. Národné zmluvy o grantoch budú zostavované v súlade s pravidlami Národného financujúceho orgánu, aj v prípade, že žiadne národné verejné prostriedky nie sú zabezpečené Radou verejných orgánov predovšetkým, čo sa týka kritérií oprávnenosti a iných nevyhnutných finančných a právnych požiadaviek, okrem prípadov kedy nie je možné vypracovať národnú zmluvu o grante z dôvodu nesplnenia národných kritérií oprávnenosti zo strany riešiteľa projektu alebo iných finančných a zákonných požiadaviek.

Finálna schválená „technická špecifikácia projektu“ vyplývajúca z rokovacieho procesu uskutočneného Spoločným podnikom bude rovnaká[6] pre vypracovanie národných zmlúv o grantoch k tomu istému projektu vo všetkých členských štátoch ENIAC.

Dátum začiatku a trvania projektu bude špecifikovaný v „technickej špecifikácii projektu“. Národné zmluvy o grantoch stanovujú oprávnené náklady, ktoré budú poskytované odo dňa začatia riešenia projektu nezávisle od dátumu ich podpísania.

[5] „Technická špecifikácia projektu“ predstavuje technický materiál, ktorý čo najjasnejšie a stručne popisuje všetky činnosti, aktivity a úlohy, ku ktorým sa účastníci projektu zaviazali a spĺňajú vedecké a výskumné ciele stanovené v zmluvách o grantoch. Východiskom je popis vedeckých/technologických cieľov a pracovných plánov načrtnutých v návrhu projektu, ktoré sa v priebehu hodnotenia a počas ďalších rokovaní o zmluve eventuálne upravia na základe špecifických odporúčaní externých znalcov. Okrem tejto jej právnej záväznosti „technická špecifikácia projektu“ slúži pre príjemcov grantu, Spoločný podnik, Národný financujúci orgán a eventuálne pre externých znalcov ako referenčný údaj, aby mohli efektívne sledovať a kontrolovať napredovanie daného projektu počas celého jeho trvania.

[6] okrem prekladov, ak je to potrebné

Národný financujúci orgán zabezpečí, aby ustanovenia národnej zmluvy o grante boli v súlade s článkom 107 odseku 1 rozpočtových pravidiel ENIAC, ktoré uvádzajú, že ak si riešenie projektu vyžaduje, aby príjemca uskutočnil verejné obstarávanie, musí požiadavku vo výberovom konaní formulovať na základe najlepšej ponúknutej ceny, t.j. vo výberovom konaní ponúkne najlepší pomer ceny a kvality, pričom sa snaží vyhnúť konfliktu záujmov.

Národný financujúci orgán vynaloží maximálne úsilie, aby urýchlil svoje interné postupy na uzatvorenie národných zmlúv o grante. Národná zmluva o grante musí byť podpísaná najneskôr do 30 dní od ukončenia rokovaní, ktoré uskutočnil Spoločný podnik (ENIAC).

Národný financujúci orgán bude informovať Spoločný podnik o podpise národnej zmluvy o grante a kópiu národnej zmluvy o grante predloží Spoločnému podniku do 15 dní odo dňa jej podpisu jej príjemcom.

Následne bude Spoločný podnik informovať Národný financujúci orgán o podpísaní zmluvy o grante medzi Spoločným podnikom a príjemcom a kópiu tejto zmluvy o grante mu predloží do 15 dní odo dňa jej podpisu.

Zmluva o grante Spoločného podniku nadobúda platnosť po pripojení sa minimálne troch neprepojených subjektov, ktoré boli založené v minimálne troch členských krajinách Spoločného podniku v deň pripojenia sa posledného z nich.

d) Technický monitoring

Spoločný podnik je zodpovedný za monitorovanie riešenia projektu v súlade s „Technickou špecifikáciou projektu„.

Konzorcium predloží Spoločnému podniku svoju technickú správu(y)[7] a výstupy v termínoch, ktoré sú na predloženie správ stanovené v „Technickej špecifikácii projektu“ a zmluve o grante uzavretej medzi Spoločným podnikom a riešiteľmi projektu.

Spoločný podnik poskytne technické správy a výsledky technického hodnotenia riešenia projektu ním vykonané Národnému financujúcemu orgánu do 15 dní po ich schválení a potvrdení výkonným riaditeľom.

Technické hodnotenie riešenia projektu vypracované Spoločným podnikom zohľadní v prípade potreby špecifické požiadavky danej krajiny navrhnuté Národným financujúcim orgánom, ktoré Národný financujúci orgán potrebuje pre akceptovanie úhrady nákladov príjemcov grantov.

Národný financujúci orgán nebude požadovať ďalšie dodatočné technické správy okrem tých, ktoré požaduje Spoločný podnik.

Správy, ktoré sú predkladané Spoločnému podniku, sú vyhotovené v anglickom jazyku.

[7] Technická správa pozostáva z prehľadu o napredovaní prác pre dosiahnutie cieľov projektu, vrátanie úspechov a dosiahnutí míľnikov a výstupov stanovených v „Technickej špecifikácii projektu“ a rozdielov medzi očakávanými a skutočne zrealizovanými činnosťami. Technická správa(y) obsahuje aj informácie o riadení (manažovaní) projektu a upravenú verziu plánov pre jeho využívanie a zverejňovanie.

e) **Finančný monitoring/Platby**

Národný financujúci orgán spracuje požiadavky na úhradu nákladov príjemcov grantov v ich vlastnom jazyku podľa vlastných postupov danej krajiny a zohľadní výsledky technického monitoringu, ktorý uskutočnil Spoločný podnik. Zabezpečí, aby boli nároky platné a náklady oprávnené a v súlade s národnou zmluvou o grante. Všetky ostatné potrebné kontrolné činnosti spadajú do kompetencie Národného financujúceho orgánu.

Prípadne Národný financujúci orgán zrealizuje platby z prostriedkov štátneho rozpočtu priamo príjemcom podľa národných zmlúv o grantoch.

Národný financujúci orgán potvrdí Spoločnému podniku výšku akceptovaných nákladov, iných finančných alebo zmluvných oblastí týkajúcich sa plnenia národnej zmluvy o grante a prípadne aj každú platbu uskutočnenú voči príjemcovi grantu. Národný financujúci orgán pošle toto potvrdenie Spoločnému podniku do 15 dní od jeho realizácie. Národný financujúci orgán zabezpečí realizáciu finančného a zmluvného monitoringu výlučne v zmysle národných predpisov a postupov.

Príslušne Spoločný podnik zrealizuje úhradu svojho príspevku príjemcom grantu do 30 dní od dňa prijatia hore uvedeného potvrdenia od Národného financujúceho orgánu.

Národný financujúci orgán bude zabezpečovať evidenciu platieb príjemcom grantov. Národný financujúci orgán obdrží informácie o príslušnom finančnom monitoringu vykonanom Spoločným podnikom.

Spoločný podnik a Národný financujúci orgán súhlasia s poskytovaním si dôkazov o platbách uskutočnených pri plnení príslušných zmlúv o grantoch predložením kópie prevodného príkazu na žiadosť druhej strany.

Každá strana upovedomí druhú stranu o prípade, že dôjde k zdržaniu alebo zníženiu platby v dôsledku neuspokojivého konania príjemcu alebo z iného dôvodu zdržania platby najneskôr do 15 dní od jeho zistenia.

5. Právo na zaplatenie

Každá strana upovedomí písomne druhú stranu hneď ako zistí, že príjemca porušil zmluvu o grante uzavretú s touto stranou ako aj povinnosť použiť prostriedky štátneho rozpočtu na vopred stanovený účel. V prípade grantov, ktoré podliehajú právu na zaplatenie, je nevyhnutné uchovávať dokumenty zodpovedajúce uplatňovaniu tohto práva (napr. dohody a záznamy o platbách) po dobu eventuálneho vymáhania.

6. Dodatky a ukončenie zmlúv o grantoch

Je v zodpovednosti každej strany upozorniť druhú stranu, že považuje jej konanie za neadekvátne a chce v platbách grantov uskutočniť zodpovedajúcu zmenu pre ich pokračovanie na základe dodatku alebo ukončiť zmluvu o grante.

V prípade že je potrebné v „ Technickej špecifikácii projektu“ uskutočniť podstatnú zmenu, Spoločný podnik bude informovať Národný financujúci orgán o účele dodatku. Národný financujúci orgán predloží Spoločnému podniku špecifické požiadavky svojej krajiny najneskôr do 15 dní od získania tejto informácie. Novú „Technickú špecializáciu projektu“ prerokuje Spoločný podnik po zohľadnení všetkých požiadaviek Národného financujúceho orgánu. Spoločný podnik oznámi Národnému financujúcemu orgánu aktualizovanú verziu „Technickej špecifikácie projektu“ do 15 dní od ukončenia tohto rokovania.

Akýkoľvek iný dodatok „Technickej špecifikácie projektu“ prerokuje Spoločný podnik, ktorý oznámi Národnému financujúcemu orgánu zmenu „ Technickej špecifikácie projektu“ do 15 dní od ukončenia tohto rokovania.

Do 15 dní je Spoločný podnik zodpovedný informovať Národný financujúci orgán o akejkoľvek zmene alebo ukončení zmluvy o grante medzi Spoločným podnikom a príjemcom.

Do 15 dní je Národný financujúci orgán zodpovedný informovať Spoločný podnik o akejkoľvek zmene alebo ukončení zmluvy o grante medzi Národným financujúcim orgánom a príjemcom.

7. Audity – kontroly

Spoločný podnik bude u príjemcov verejných finančných prostriedkov Spoločného podniku uskutočňovať kontroly na mieste a finančné audity. Tieto kontroly a audity bude vykonávať buď priamo Spoločný podnik alebo Národný financujúci orgán v mene Spoločného podniku na základe žiadosti Spoločného podniku. Národný financujúci orgán môže na vykonanie kontrol a auditov menovať externý orgán, ktorý tak urobí v jeho mene. Národný financujúci orgán je oprávnený uskutočniť u príjemcov prostriedkov štátneho rozpočtu iné kontroly a audity, v prípade že to považuje za nevyhnutné a Spoločný podnik oboznámi s ich výsledkami.

Obidve strany sa budú vzájomne informovať o začatí ako aj o výsledkoch všetkých kontrol a auditov ustanovených v zmysle predchádzajúceho odseku, a to do 15 dní.

8. Politika práv duševného vlastníctva

Pre účely národných zmlúv o grantoch v rámci tejto zmluvy a bez toho, aby boli dotknuté pravidlá hospodárskej súťaže Spoločenstva, prednosť majú ustanovenia o duševnom vlastníctve schválené Nariadením Rady (EK) č. 72/2008 pred vnútroštátnymi predpismi, pravidlami o poskytovaní grantov alebo projektami súvisiacimi s duševným vlastníctvom.

9. Dôverné informácie

Všetky informácie, ktoré príslušná strana získa v súvislosti s touto dohodou, sa budú považovať za dôverné a každá strana súhlasí, že:

(a) bude dôverné informácie chrániť zodpovedajúcim a adekvátnym spôsobom v súlade s platnými odbornými štandardami;

(b) bude dôverné informácie používať a reprodukovať len na účely stanovené v tejto dohode;

(c) nebude zverejňovať alebo iným spôsobom poskytovať dôverné informácie iným osobám ako tým, ktoré tieto informácie potrebujú na splnenie účelu stanoveného v tejto dohode.

Predchádzajúci odsek sa nebude vzťahovať na informácie,

(a) ktoré sú verejne známe; alebo

(b) ktoré prijímacia strana už pozná;

(c) keď je zverejnenie dôverných informácií požadované národným zákonom.

10. Administratívne záležitosti

Zúčastnené strany tejto dohody si budú uchovávať a aktualizovať zoznam kontaktných osôb zodpovedných za vybavovanie záležitostí týkajúcich sa tejto dohody.

Obidve strany sa budú vzájomne informovať o iných osobách, ktoré sú zodpovedné za príslušnú uzavretú zmluvu o grante.

Kompletná komunikácia medzi stranami sa uskutočňuje v anglickom jazyku[8].

Kompletná písomná komunikácia medzi zúčastnenými stranami tejto dohody bude prípadne uvádzať názov zmluvy a identifikačné číslo (Národného financujúceho orgánu /alebo Spoločného podniku). Každá strana bude druhej strane odpovedať na otázky týkajúce sa tejto dohody najneskôr do 7 pracovných dní. V prípade, že druhá strana nedostane žiadnu odpoveď ani do 15 dní, bude sa to považovať za kladnú odpoveď.

11. Práva kontroly Európskej komisie, OLAF a Dvora audítorov

V súvislosti s touto dohodou zabezpečia obidve strany uplatňovanie kontrolných práv Európskej komisia, Európskeho úradu pre boj proti podvodom a/alebo Dvora audítorov podľa článku 12 odseku 5 a článku 12 odseku 6 Nariadenia rady (EK) č. 72/2008.

12. Riešenie sporov

Súd prvého stupňa alebo odvolací súd, Súdny dvor Európskych spoločenstiev má výlučnú súdnu právomoc pri riešení súdnych sporov medzi Spoločným podnikom a Národným financujúcim orgánom, ktoré sa týkajú výkladu, uplatnenia alebo platnosti tejto dohody.

13. Trvanie dohody

Táto dohoda nadobudne platnosť v deň jej podpísania oboma stranami dohody a bude platná počas obdobia členstva Slovenskej republiky v Spoločnom podniku. Túto dohodu možno kedykoľvek meniť na základne vzájomného písomného súhlasu zúčastnených strán. Táto dohoda nezahŕňa teraz alebo

[8] V prípade, že je nevyhnutné podpísať pôvodné materiály, ktoré Národná grantová organizácia vyhotovuje v domácom jazyku, Národná grantová organizácia ich predloží spoločne s prekladom do anglického jazyka.

v budúcnosti žiadnu výmenu finančných prostriedkov, ani vytvorenie akéhokoľvek záväzku voči časti akejkoľvek strany na vykonanie úhrady voči inej strane.

Táto dohoda pozostáva z úplnej dohody uzavretej medzi zúčastnenými stranami na stanovený účel a jej úpravy alebo dodatky platia len po uvedení a priložení podpisov obidvoch strán tejto dohody.

Vyhotovené v Bruseli v dvoch kópiách

za Spoločný podnik

vlastnoručný podpis

Dirk Beernaert

dočasný výkonný riaditeľ

za Ministerstvo školstva Slovenskej republiky

vlastnoručný podpis

p. Marta Cimbáková

riaditeľka odboru štátnej a európskej politiky vo vede a technike

Úsek vedy a techniky

ENIAC JOINT UNDERTAKING

TECHNICAL ANNEX

E^2COGaN – Energy Efficient Converters using GaN Power Devices

ENIAC Call 2012 – 1

1 ESSENTIALS

Project acronym	E^2COGaN
Project full title	Energy Efficient Converters using GaN Power Devices
Sub Programme, in order of importance	3. Energy Efficiency 3.2 Energy Distribution and Management – Smart Grid Energy Efficiency >> 90% (solar inverter / EV battery charger) 1.1 Intelligent Electrical Vehicle Energy efficiency and CO2 reduction through smart interconnections 3.1 Sustainable and efficient energy generation Energy efficiency >> 90%, reliability and lifetime (solar inverter) 8. Equipment, Materials and Manufacturing 8.2 More than Moore GaN power technology addressing new functionalities
Version of Technical Annex	TA version 1.0
Date of Technical Annex	29/11/2012
Start Date of Project	01/04/2013
Duration of project	36months
Maximum JU funding	3,940,787.00€
Coordinator	ON Semiconductor Belgium BVBA
Project coordinator	Frederik Deleu
Tel	+32 55 332932 / +32 499 596103
Email	frederik.deleu@onsemi.com

2 HISTORY OF TECHNICAL ANNEX LATER ANNEX 1 TO THE JU GA

Version Number	Date	Main changes / Amendment number	Description
0.1	*15/11/2012*	*First draft*	*Copy of FPP into TA template; apply changes of coordinator, WP2 leader, DEA-LETI contribution;*
0.2	*23/11/12*	*Minor changes*	*Change contribution of NXP-B to WP7; add explanation to table 2; add explanation on resource section*
0.3	*27/11/12*	*Content update*	*State-of-the-art updates, standards and IP management.*
0.4	*28/11/12*	*Content update*	*Complete specification table, add information on subcontract cost, add comment about standards.*
1.0	*28/11/12*	*End of negotiations*	

3 PUBLISHABLE PROJECT SUMMARY

Efficient power conversion systems are at the heart of the worldwide effort for a green economy, since they can minimize losses and save energy and contribute thus to achieve a better CO_2 balance sheet. Semiconductor power devices are a central part of any power conversion circuit and are ubiquitous in our daily lives: they transform voltages for a multitude of appliances, such as from the 220V AC mains to a 12V DC end-user appliance and enable to convert from DC (such as a battery in an electric car) to AC (such as a motor drive) and vice versa. The importance and the key role of power conversion systems are especially significant in cases where operation relies on battery or limited renewable energy sources where they are a key element of the overall efficiency of the system. Hence, highly efficient power switching devices are a key for successful introduction of full electric vehicles into the market.

Traditionally, high voltage (>400V) power switches are made in silicon. Several major breakthroughs in silicon power device architectures have been accomplished (IGBT, super-junction) over the past 30 years. However, due to the intrinsic properties of silicon (relatively low bandgap, limited thermal conductivity, etc), advances have slowed down. Further performance improvements and higher efficiencies will become more and more challenging and cost-intensive to achieve. This is the driving motivation why the industry is currently investing in the research and development of disruptive power device technologies, as based on the Wide-Band Gap (WBG) materials GaN and SiC, to replace the incumbent Si technologies with the mission to achieve a higher performance at equivalent cost.

Both SiC and GaN present a band gap of about 3.3eV and an associated critical field of about 3 MV/cm – 10 times higher than in Si – enabling to decrease considerably the total chip area at equivalent high voltage and on-state resistance. The current designs mainly rely on unipolar structures (FET-based switches and Schottky-barrier diodes) having very low switching losses and practically no reverse recovery energy. These properties allow stepping the switching frequency to higher levels, enabling a massive reduction of passive elements like inductors and capacitors. The wide band gap also makes WBG-based devices intrinsically interesting for the use in harsh environments under high temperatures, making them a strong contender for the automotive market. SiC diodes are for instance commercially available, with the first switches being currently introduced. SiC power electronics is however still hampered by a severe cost penalty of the SiC starting material.

Boosted by the widespread use of GaN in optoelectronics – GaN is the starting material for blue and green emitting (laser) diodes – GaN electronic devices have been developed starting from radar and RF for military and aerospace applications. Recent advances in the challenging epitaxy of GaN on silicon starting substrates triggered the investigation of GaN for the high volume market of power conversion.

The advances in the GaN-on-Si technology promise for the first time to bring down the cost of a high-performance wide-band-gap power technology to silicon cost level. We foresee a dominant position by the end of this decade in power converters for electrical vehicles and photovoltaic systems.

This project will target the demonstration of GaN-on-Si as a disruptive High Voltage (HV) technology (Schottky Barrier Diodes (SBDs) and High Electron Mobility Transistors (HEMTs)) through the whole value chain up to demonstrators with high industrial, societal and environmental relevance. More precisely the character will be proven through a well-balanced and application specific trade-off between the "corner" benefits given by higher efficiency, higher switching frequency, smaller footprint and weight and competitive cost on system level with respect to Si or SiC. The consortium is set up in order to provide a common and global, industry-relevant approach implying the whole GaN power electronics value chain from the substrate provider, GaN device manufacturer, assembly house to the end user, completed by

top academic institutes and other tool or service providers (simulation software, measurement tools, etc.). Concerning the GaN power devices the plan is to start with 600V, 10A and gradually explore higher voltages (up to 1500V) and currents (up to 100A) towards the end of the project, giving priority to the early exploration of applications below 10kW.

Special attention will be paid on reliability issues and parasitic effects that will be investigated through a combined approach based on advanced electro/optical measurements and electro/thermo/mechanical TCAD simulations allowing to understand and identify the Safe Operating Area and to develop a robust and reliable GaN-on-Si power device technology platform.

Another important topic is the development of suitable packages / modules allowing high frequency and/or high temperature operation together with the design and implementation of the associated gate drivers.

Finally, the project demonstrators will focus on two application domains with strategic relevance:

First, on Photovoltaic (PV), where the use of GaN will be explored in micro-grid interfacing circuits evaluating an overall gain in system efficiency and operating cost over incumbent Si- or competing SiC-based solutions.

Second, on Automotive, where the benefit of GaN will be investigated in grid-connected chargers for high voltage batteries, as found in new hybrid and full electric vehicles. Power conversion for interfacing to lower voltage levels will also be investigated. Main motivations are gain in efficiency, weight, footprint and – related to the expected high temperature operation capacity – ease in the heat and cooling management.

Moreover, the project will include a pre-study in Aeronautics with specific high temperature (250°C) mission profiles as well as the atmospheric radiation constraint.

Among the foreseen potential societal and environmental impact of this project are the establishment of a pan-European GaN power electronics technology ecosystem and competence ensuring the autonomy of Europe on strategic and disruptive semiconductor and power conversion technologies, the contribution to higher efficiency in both energy generation and usage and last, but not least, a significant step towards a knowledge-based, resource efficient, low carbon European industry and economy.

4 RELEVANCE AND CONTRIBUTIONS TO THE CONTENT AND OBJECTIVES OF THE CALL

One of the EU's major goals for 2020 is to cut the CO_2 emissions of more than 20% with respect to 1990 values, while ensuring a sustainable growth based on a knowledge-based economy. This implicitly requires a resource-efficient industry, which is one of the major EU challenges for the beginning of the 21st century.

In order to reach this objective of a resource-efficient industry, private and public actors have to review the whole chain of energy generation (including thus a high proportion of renewable energies), distribution (e.g. via smart grids) and storage (e.g. batteries) and find new ways and technologies to avoid losses where ever possible. Very much related, electrical transport will need to be built out in order to replace or reduce the use of a low-efficient combustion engine by more efficient and cleaner sources of energy.

A crucial element in the overall energy efficiency is the efficiency of the power conversion steps. Power conversion is omnipresent all the way from the electricity provider to the end consumer and occurs basically at any utility interface. To give two examples, which are also chosen as demonstrators in the E²COGaN proposal: power conversion will ensure the energy injection from solar modules into the grid via a DC/AC converter and power conversion will allow us to charge the battery of an electrical vehicle via an appropriate converter once connected to the mains.

Due to the multitude of power conversion steps along the distribution chain, the gain of 1% in efficiency at one level can already make a huge difference in the overall efficiency of the system.

So far, technologists lacked a solution that could give a good trade-off between performance and costs along the value chain from die to system level. Silicon high voltage devices (IGBTs, Superjunction) are reasonably priced, but have already reached their performance scalability limit. For what concerns SiC power devices, they have already shown their potential of higher efficiency for both diodes and transistors, but prices are high and are not likely to decrease in the near future due to the expensive substrates, thus hindering a broader market entry and wider use.

In this respect, GaN power devices can be seen as a revolutionary technology: they have the unique potential to combine both an appealing price roadmap –GaN starting substrates will decrease in price with the optimization of GaN growth on Si using multi-wafer epitaxy tools while device production will be carried out in conventional silicon manufacturing lines – and high performances being equal or better to state-of-the-art SiC devices in the 600V -1200V range and by far better than incumbent Si technologies on die level. Regarding the final applications at the top of the value chain, further advantages appear related to their capability of higher switching frequencies and higher temperature operation. Application designers will thus be able to reduce the size of passive components needed on system level (such as inductors and capacitors) or even the cooling requirements, giving benefits in terms of system cost and foot print thus enabling further integration.

In this project we will demonstrate the high potential of GaN power devices through the whole value chain up to relevant applications with societal impact: in photovoltaic via inverters with higher efficiency and lower cost, in automotive via battery chargers and HV/LV DC/DC converters with compact and cost effective design.

More precisely, this proposal will provide relevant solutions to 3 of the 8 domains and 4 of the 25 grand challenges as listed in the latest Annual Work Plan (AWP) 2012: to the Grand Challenge 1 "Intelligent vehicle" of Domain 1 "Automotive and Transport", to the Grand Challenges 1 "Sustainable and efficient energy generation" and 2 "Energy distribution and management – smart grid" of Domain 3 "Energy Efficiency" and finally to Grand Challenge 2 "More than Moore" of Domain 8 "Equipment, Materials and Manufacturing".

The E²COGaN project has the highest compliance level with the Grand Challenge 3.2 “Energy Efficiency - Energy distribution and management – smart grid” which covers thematically the main GaN-device based application demonstrators such as the solar inverter – feeding electricity into the grid – and the electric vehicle battery charger – storing the electricity provided by the grid for further use in transport.

Moreover, the E²COGaN project has a high compliance level with the Grand Challenge 1.1 “Automotive and Transport – Intelligent Vehicle” mapping out new ways of enabling technologies for electric cars in terms of highly efficient battery charging and overall power management. It is also strongly related to Grand Challenge 3.1 “Energy Efficiency - Sustainable and efficient energy generation” aiming to achieve higher efficiency solar inverters based on GaN power devices while including cost aspects and lifetime constraints, contributing thus to reduce the overall losses between the generation of renewable energies and its usage by the end customer.

The project furthermore contributes to a sustainable European semiconductor industry for the globalization era: GaN devices as an emerging technology with increasing world-wide demand will be produced in existing European 6” and 8” Si production facilities whose existence otherwise would be threatened by the gradual out-phasing of incumbent silicon technologies (moving to larger wafer sizes or even ceasing production) making thus the best use of existing European manufacturing infrastructure in terms of facilities, tools and competences, which is completely in line with the Grand Challenge 8.3 “Equipment, Materials and Manufacturing - More than Moore”.

5 R&D INNOVATION AND TECHNICAL EXCELLENCE

Efficient power conversion systems are at the heart of the worldwide effort for a green economy, since they can minimize losses and save energy and contribute thus to achieve a better CO_2 balance sheet. Semiconductor power devices are a central part of any power conversion circuit or module and are ubiquitous in our daily lives: they transform voltages for any kind of appliances, such as from the 220 V AC mains to a 12 V DC end-user appliance and enable to convert DC (such as a battery in an electric car or PV modules) to AC (such as a motor drive and grid) and vice-versa (in the case of chargers). The importance and the key role of power conversion systems are especially significant in cases where operation relies on battery or limited renewable energy sources where they are a key element of the overall efficiency of the system.

The general concept of this project is to develop the next generation of power electronic devices based on a scalable, cost-effective, high-performance and reliable GaN-on-Si device technology platform which will provide discrete and integrated devices suitable for 600 V and higher (up to 1.2 kV) and to prove its benefits at application level in photovoltaic systems and full electric vehicles. To be successful, the complete value chain from wafer suppliers, IDMs, module makers to end-users has to be considered involving competences from large industrial partners, SMEs and institutes and academics. The project aims to validate the emerging and revolutionary GaN HV technology from wafer levels to relevant end products thus putting Europe at the forefront of both energy efficient power conversion efforts and an innovative GaN power electronics ecosystem.

5.1 GaN-on-Si Power Devices

(a) State of the art

The specific on-resistance R_{ON}*A as a function of breakdown voltage V_{BD} is the most widely used figure of merit to characterize the device performance since it determines the conduction losses and to some extent the switching losses of the device. Generally speaking, lower R_{ON}*A leads to more efficient devices suitable for operation at higher frequencies. A summary of the state of the art results for GaN is given Figure 1.

The first thing to notice is that in terms of materials parameters, GaN is theoretically superior to all other competitor devices. As today, SiC seems to be more suitable for voltages higher than 1000 V while GaN is more suitable for voltages below 1000 V presenting the advantage of lower R_{ON}*A at equivalent V_{BD}. It is interesting to note that the best results are obtained with GaN devices grown on sapphire substrates (triangle symbols) featuring **state of the art values of R_{ON}*A ~1 mΩcm^2**.

Furthermore, GaN shows excellent switching behaviour in Schottky diodes (Q_{RR} comparable to that of SiC) and in GaN HEMTs (the switching charge Q_{GD} being 10 times smaller than in a comparable Si device).

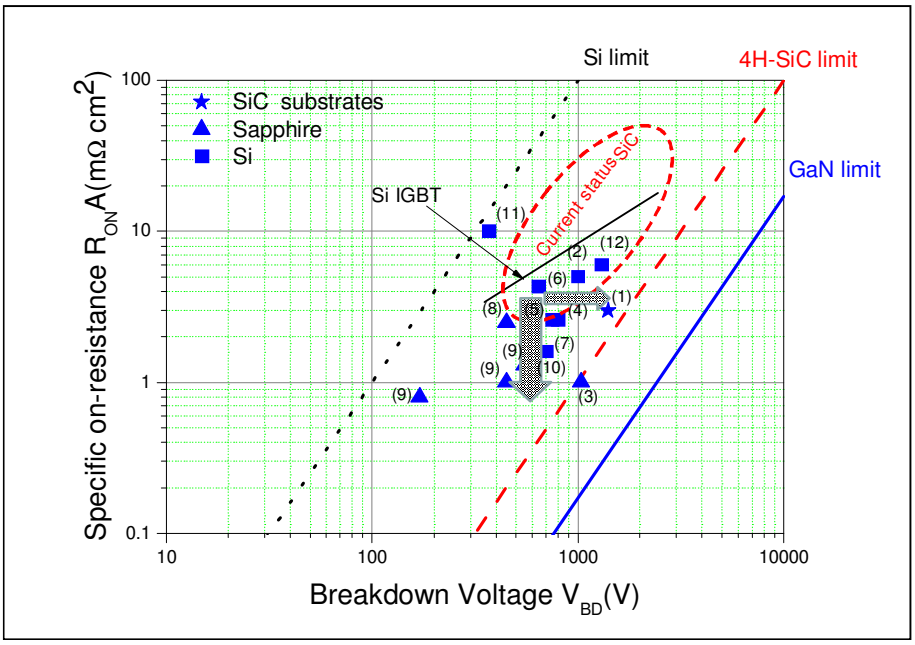

Figure 1: Summary of the state of the art RON vs VBD. The symbols represent experimental results for GaN HFET devices on different substrates Si(■), Sapphire (▲) and SiC (*).The lines represent the theoretical limits for Si, SiC and GaN devices determined from fundamental materials properties. The dashed ellipse represents the current status of SiC devices. The thick and thin arrows represent the project target towards lower R_{ON} and higher V_{BD}, respectively.

However, many issues still remain and have to be understood and solved in a concerted manner before aiming any market introduction. Unless using an insulated gate, GaN HEMTs tend to be leaky (I_{OFF} = 100 µA/mm) compared to Si devices. Also, they are sensitive to self-heating due to their comparatively small size and large current density. Moreover, the complex epitaxy structure forming the HEMT device is sensitive to trapping phenomena in the different layers or their interfaces that can influence the switching behaviour (gate or drain lag) or even degrade the basic device parameters (R_{ON}, V_T, I_{ON}, I_{OFF}). As a wide band gap material, GaN is considered to bring higher temperature robustness, but this will need to be proven on realistic HV devices.

In addition, most of the work focus is on GaN devices at voltages around 600 V which fulfils the requirements for several power applications; only very few reports have demonstrated devices operating higher than 1000 V. Moreover, most of the reported results have been obtained on wafer sizes of 100mm or smaller and based on III-V process integration flows, This, however, is incompatible with the objective of low-cost, high volume manufacturing to achieve maximum market penetration, that will require larger wafer sizes (150 or even 200mm) and the best use of existing silicon production know-how and facilities. Finally, most of the work presented in Figure 1 describes device performance characteristics without systematic reliability studies. All of the aforementioned call for further improvements to take full advantage of GaN potential superiority.

However, despite all the promising performances, the AlGaN/GaN power devices still suffer from various limiting factors that can be grouped as: i) parasitic and ii) reliability issues. These parasitic and reliability aspects have not yet been largely investigated. In particular, the multiple effects of highly energetic carriers (hot-electrons), high electric field and high power densities, present within the device active area, require an in-depth investigation and understanding in order to design and to develop a robust and reliable GaN device platform.

(b) Advances beyond the state of the art

Figure 1 shows how GaN can be improved significantly at least up to the theoretical limit (thick solid line). This would require large efforts aiming to decrease R_{ON}*A and to simultaneously increase the breakdown voltage. Here in this project we will mainly focus on the improvement of R_{ON} *A (thick vertical arrow) for 600 V devices devoting also a smaller exploratory effort toward higher voltages up to 1500 V (thin horizontal arrow). Aim is to maintain good performance or even advances beyond the state of the art while extending the technology to large area up to 200 mm Si wafers in CMOS compatible process. To achieve this, the material quality will be improved through epitaxy, Au-free contacts and normally-off enhancement mode architectures.

In addition, to exploit the full potential of GaN HV devices while challenging incumbent Si and competing SiC technologies, it is mandatory to provide both a deeper and broader look on their intrinsic and parasitic physics and understand how it relates to potential use in applications. A considerable effort of the E^2COGaN project will be spent to provide these answers through all kinds of electrical characterizations on wafer, packaged device and module level via DC and AC measurements, but also complementary and innovative analysis techniques such as IR for thermal mapping, DLTS for trap density and energy level scanning and electroluminescence for mapping of hot electrons. This will be complemented with reliability investigations.

5.2 Power Module Assembly and System Integration of GaN Power Devices

(a) State of the art

Classical Si power devices consist of a top side die contact realised with Al-wire bonds and a backside contact to the ceramic substrate (i.e. DBC) realised with solder (see Figure 2). The ceramic substrate itself is bonded to the base plate of the module, which is filled with an encapsulant (i.e. silicone). In the end application the module is mounted to a water cooler, where the thermal contact is enabled by a thermal interface material (TIM, i.e. grease, paste, foil, pad …).

R&D on packaging of power devices has been mainly challenged by achieving good electromagnetic compatibility and good thermal heat dissipation in order to reach good system performance, while price and size need to be kept in a reasonable range. At the same time the package needs to deal with different coefficients of thermal expansion (CTE) of the materials used for packaging. Due to the varying loads leading to many temperature changes this issue is the main limiting factor to achieve long lifetimes.

Consequently current R&D activities are focussed on finding new technologies in order to reduce thermal resistance and increase the life time.

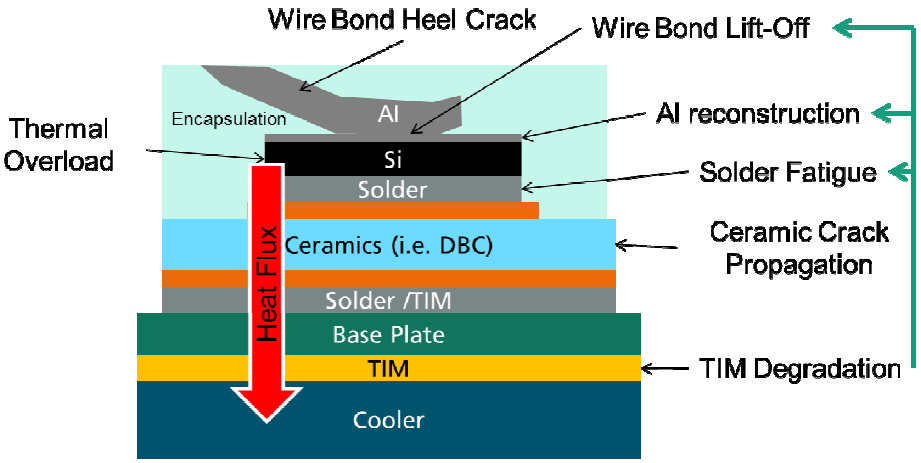

Figure 2: Classical structure of a power module with indication of the main heat path and failure mechanisms.

Besides the assembly of the power devices the gate control has an important influence on the overall efficiency of a power module. GaN power devices offer new perspectives in converter efficiency with at the same time challenging requirements for the gate driver.

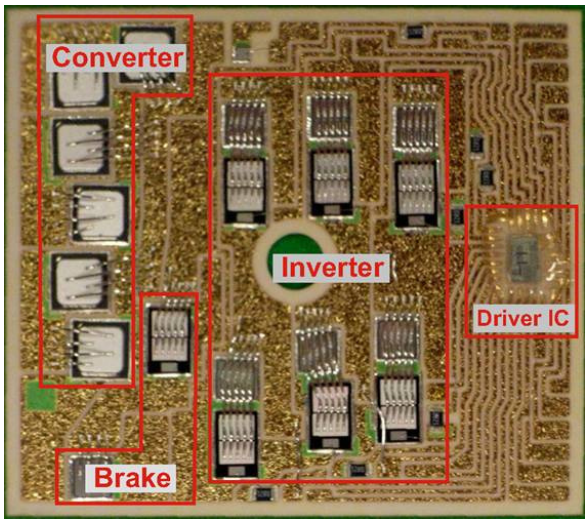

Figure 3: Example for system integration in a module today: A 3-phase rectifier bridge (converter: 600V Si-diodes), a 3-phase inverter (600V Si-IGBT and freewheeling diodes (FWD)), a brake-chopper (600V Si-IGBT and FWD), the gate-driver for all 7 switches and several sensors and SMD-components are compact assembled (soldered and bonded) on a ceramic substrate in a module with excellent cooling. (Semikron)

Many gate drivers are available today for power MOSFETs but they are not sufficient to drive GaN power devices. Special characteristics of GaN devices like fast switching characteristics and resulting high dV/dt, low threshold voltages for enhancement mode GaN devices and reduced maximum rating for the gate driving level require dedicated GaN drivers and an adapted module design. Also the intended increase in switching frequency requires optimized gate drivers and additional measures in board design to further decrease parasitic capacitance and inductance.

Fig. 1 shows an example for the state of the art system integration with Si- devices today. In the project the Si power devices (diodes, switches) should be replaced by

corresponding GaN-HEMT devices in a cascode topology with low voltage MOSFET in series and a freewheeling-diode in parallel and the whole assembly and the gate driver have to be adapted or developed to the needs of GaN devices.

(b) Advances beyond the state of the art

In comparison to Si devices, GaN devices impose new possibilities and boundaries, which need to be explored. They enable the operation at high temperature conditions and higher switching speeds. Thus packaging is becoming the limiting factor. Classical solders do not withstand high operating temperatures and new approaches need to be evaluated in their feasibility (i.e. silver sintering, transient liquid phase bonding, etc.). Additionally the classical challenge of different CTE's will be even more severe. Thus the project is focused on the application of new interconnect technologies and new designs for reduced size and thermo-mechanical stresses. These approaches need to be designed, realised, evaluated and tested in order to achieve sufficient performance and lifetimes.

New concepts will be evaluated, because GaN devices are planar, which means that there is no current flow from top to bottom like in vertical Si devices. Therefore electrical contact is done from only one side of the chip. This enables alternative packaging constructions (i.e. Flip-Chip), which can give benefits to the thermal and electrical behaviour of the packaged device.

GaN enables operation at higher temperature and higher switching frequencies which demand for alternative module construction with assembly of the driver chips directly inside the module. This provides minimal parasitic inductance and capacitance between the driver and the GaN power transistors. This requires high temperature capable gate driver circuitry in order to benefit from the extended temperature capability of GaN power devices. In addition these high temperature capable modules also enable applications with high ambient temperatures up to 250°C, like they are required for example in aeronautics, which is not accessible with standard CMOS bulk technologies. Final objective is to perform a complete validation of the power electronic system in terms of the inverter topology, isolation, driver and monitoring circuitry, sensors, cooling and high T/harsh environment reliability. System design and packaging issues will also be addressed and benchmarking with respect to Si and SiC will be performed.

Therefore this work will focus on a complete system innovation, which brings together the following tasks and expertises:

- Electrical system design including high temperature (250°C) gate drivers
- Package design supported by modelling (thermal, thermo-mechanical)
- Packaging technology and module assembly: "standard assembly" (soldering or gluing + thick wire bonding, flip chip technology) and new low temperature sinter assembly technology of GaN devices for higher operation temperatures and higher reliability etc.
- Advanced reliability testing
- Application circuit development for GaN devices
- Development of gate driver and monitoring circuits and their integration with high voltage isolation and for high temperature operation respectively
- Module demonstrators using conventional and novel topologies for different power system applications, e.g. inverters for industrial drives, power supplies, automotive and photo voltaic.
- System integration of GaN power devices, insulation and cooling, driver and sensor functions.

5.3 Selected end-user applications using GaN power devices

(a) State of the art

In this project the focus will be on two end application domains where GaN-based power devices are predicted to change to product landscape in the near future: photovoltaic and automotive. Both areas are interesting for their high volume market perspectives as well as for their specific technological challenges that might be overcome by making best use of the key features of GaN power devices.

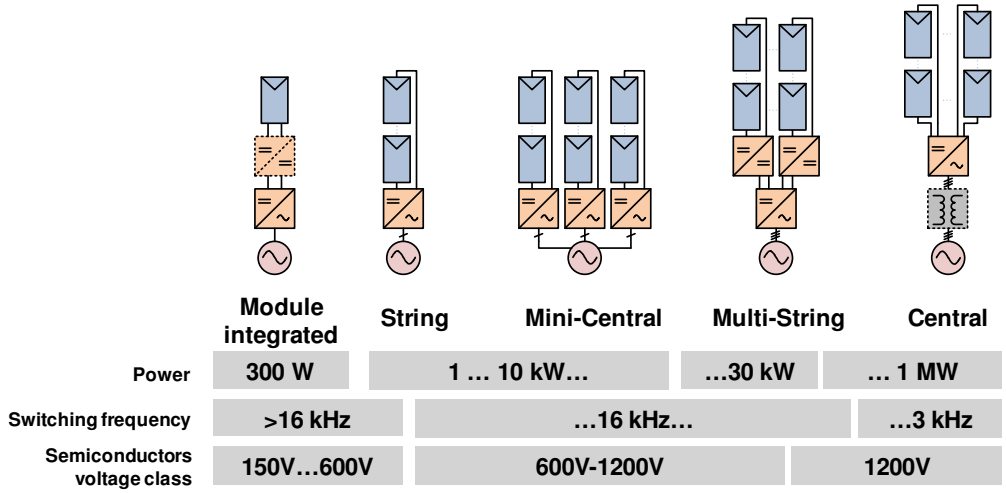

Figure 4: Grid connected PV system approaches and their corresponding frequency and power ranges.

In Photovoltaic (PV), we observe a multitude of possible approaches concerning the array arrangement and the power conversion circuit properties as illustrated in Figure 4. This offers a diversified market where the introduction of new technologies can be performed in gradual steps going from lower to higher power levels, as chips with higher current ratings become available. As today, the most commonly used semiconductor technologies in PV power conversion are Si-IGBTs, Superjunction MOSFETs (up to 600V) and - in new designs - to a certain extent SiC-diodes.

One of the key driving elements in the development of PV converters is the steady quest for higher efficiency levels (cf. Figure 5). These can in return be directly translated in lower installation costs (as fewer modules are required to produce the same energy) and faster payback time. Figure 5 shows an overview of the evolution of the efficiency levels of commercial products and R&D prototypes over the last ten years. Using SiC, spectacular levels of efficiency (99%) have already been achieved, but in many cases at prohibitive cost (e.g. by over sizing the active devices).

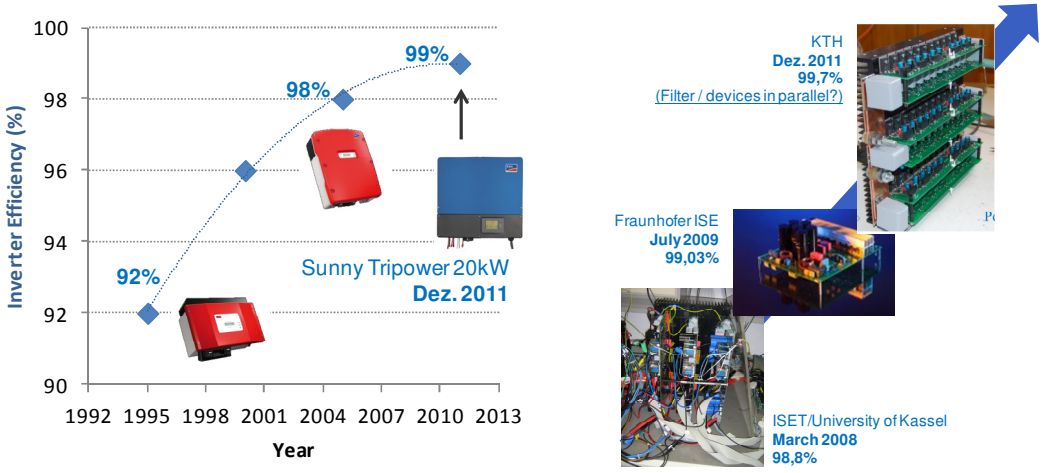

Figure 5: Grid efficiency development of commercial products and in R&D.

The real challenge is therefore to achieve very high levels of efficiency at an affordable, Si-comparable price – or better - below. Indeed, in the past there has been a pronounced trend towards continuous cost reduction of solar power inverters and modules. But still today, one can observe a significant price discrepancy between PV and motor drive inverters, especially at lower power ratings, demonstrating the remaining potential for cost reduction (cf. Figure 6). Another important challenge is the increase of reliability and elimination of failure modes of the power electronics system assuring low maintenance costs and stable and reliable grid supply.

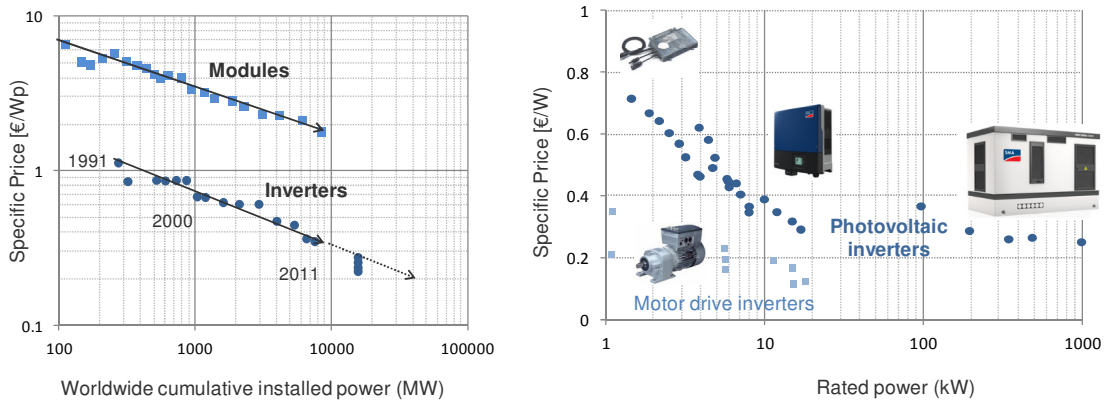

Figure 6: PV inverter and module "learning curves" and comparison of the specific price as a function of power rating for PV and motor drive inverters.

Figure 7 shows the cost break down of a PV inverter system. Only 12% of the system cost is directly linked to the power electronic components themselves. However, a smart choice of the power electronic components can have a significant impact on the expenditure on magnetic components and finally also the enclosure of the system, both elements being responsible of as much as 30% of the system cost as today. As illustrated in Figure 7, an increase of the switching frequency by a factor 4 enables a reduction in size (and cost) by approximately the same factor of the magnetic components.

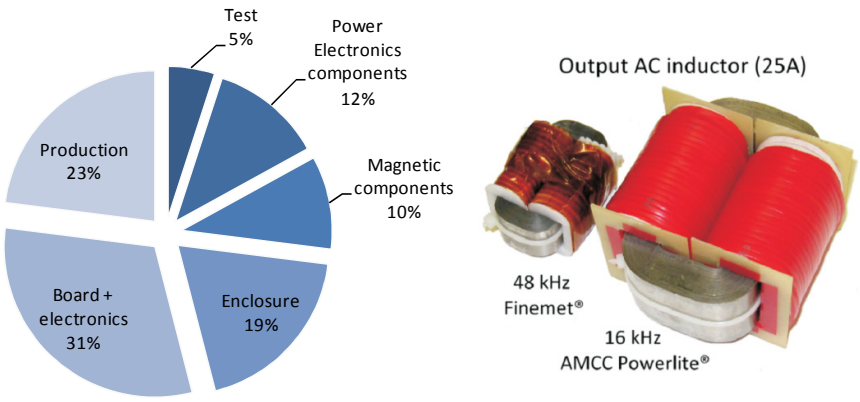

Figure 7: Cost breakdown of PV inverters and possible size savings in filter inductors due to higher switching frequencies.

Also the cooling requirements play a very important role in the overall cost structure. When using high efficiency devices having very low heat dissipation and/or devices capable to operate at higher junction temperatures, designers can admit higher thermal resistances in the assembly, which gives access to immediate cost savings on system level as illustrated in Figure 8.

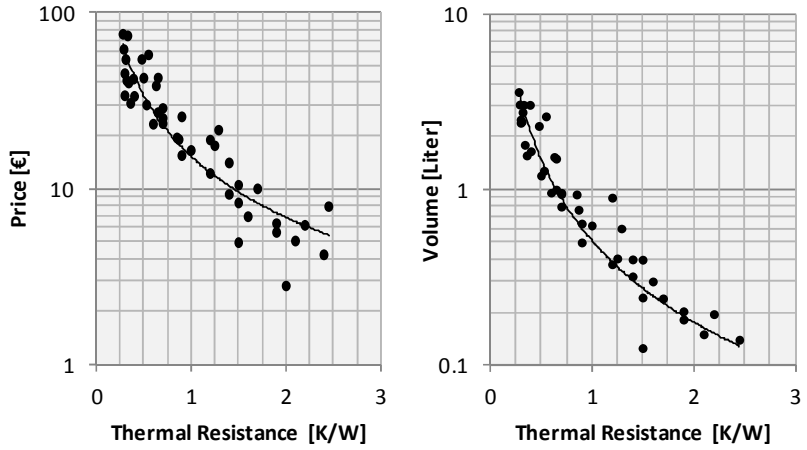

Figure 8: Price and volume of passive cooled heatsinks as a function of thermal resistance values.

Automotive applications, more specifically the multitude of power conversion systems used in novel hybrid and full electric vehicles, represent the second field of applications considered in this project to validate the GaN power device technology. As illustrated in Figure 9, the main characteristics and design targets are the extreme high levels of power density given size and weight constraints in transportable systems.

An overview of common conversion system concepts used in hybrid and full electric automotive applications together with the corresponding specifications is presented in Figure 10. Also in automotive, Si-IGBTs and Si-Diodes are the workhorses for most of the power conversion applications. Superjunction-MOSFETs are mainly applied at lower power levels (below 4kW). SiC diodes start to appear in some applications: used as freewheeling diodes parallel to Si IGBTs they can be used to improve the overall efficiency of conventional Si-based inverters to a certain extent.

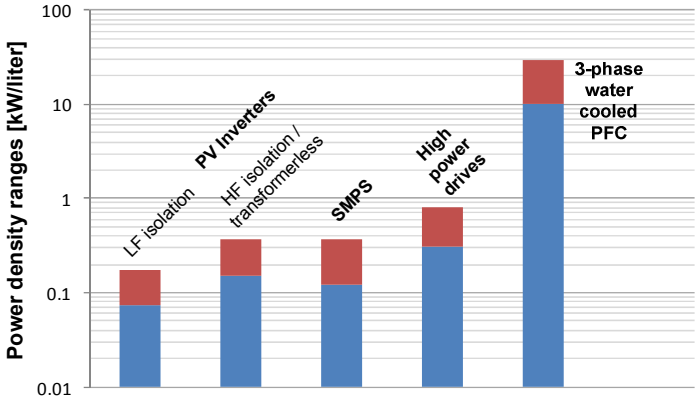

Figure 9: Comparison of power density levels for different power conversion applications

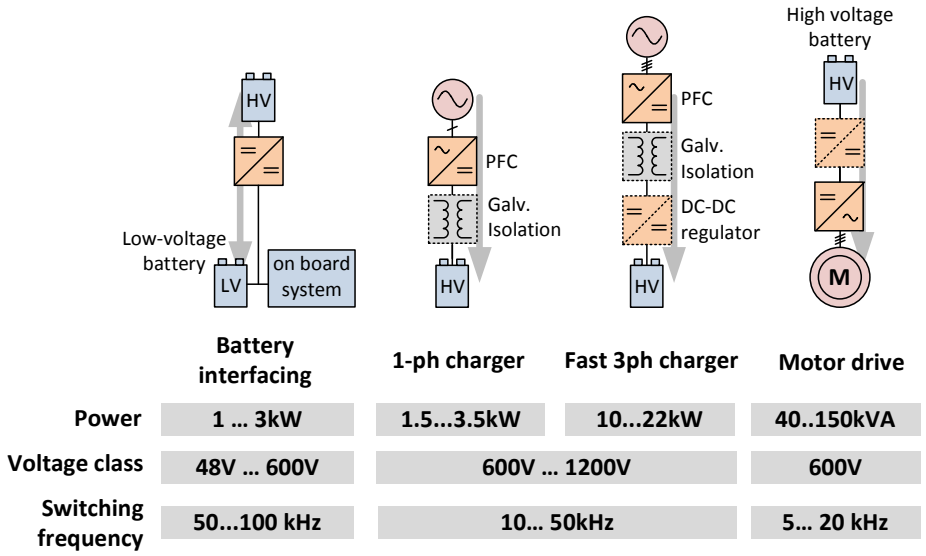

Figure 10: Overview of automotive main power conversion systems

These different conversion systems require different optimization approaches. Regarding the drive train, a high power density is less critical given the absence of output filters. As a consequence, the switching frequency is kept within a minimum level (linked to the engine rotation) in order to minimize losses in both semiconductor devices and the electric motor. Here, the reduction of losses in and the size of the power devices rather than high frequency capability will be the right criteria of choice of a new power device technology. Also operation at higher values of junction temperature (beyond 175°C) will be an asset: it lowers the cooling requirements and prevents from over sizing the converter, sometimes applied to deal with the limited temperature range. Within the E^{2}COGaN project, the automotive inverter will be deemphasized as a demonstrator target as we do not regard as the most likely GaN power device target application.

So far, the more interesting applications are charging circuits for high voltage batteries with galvanic isolations. Here the combination of high frequency switching, low losses and high temperature capability is largely preferable to achieve an optimal design, featuring compactness, a simplified cooling system and high efficiency. The same properties would

also be beneficial for in DCDC power conversion for interfacing the high voltage battery pack to the 12V board net. Both applications therefore have been chosen as main demonstrator targets to validate the outcomes of GaN technologies at a system level.

(b) Advances beyond the state of the art

It has already been shown in literature that GaN power HEMTs have only 10% of the gate-drain capacitance for the same on-state resistance compared to Si power MOSFETs. As a consequence, the energy loss per switching event is by far lower than in a Si device. Similarly, GaN Schottky Barrier Diodes (SBDs) are by far more efficient than their Si counterparts due to the quasi-absence of reverse recovery charges. This reduction of the energy loss per switching event is – as stressed in Figure 11 - a key enabler for high frequency switching while not compromising the overall efficiency: to gain a factor of 10 in frequency, the energy loss has to be decreased by the same multiplier in order to enable and maintain the same efficiency level in the final application.

Nevertheless, a series of developments is still needed in order to reach the intrinsic potential of GaN power devices on system level. Very critical is an intelligent design of the package and/or module with low inductive commutation path (to limit the overvoltage) and low coupling capacitance to the package (to limit common mode currents). Directly connected with such developments is the necessity for new PCB (printed circuit board) design techniques focusing not only on low parasitics, but also on low electro-magnetic-emissions. As such tasks become increasingly difficult when moving in the direction of higher current ratings (due to paralleling), the option investigated inside the project, will be the external parallel connection by magnetic means which is expected to offer additional voltage levels in comparison with with natural interleaving technique.

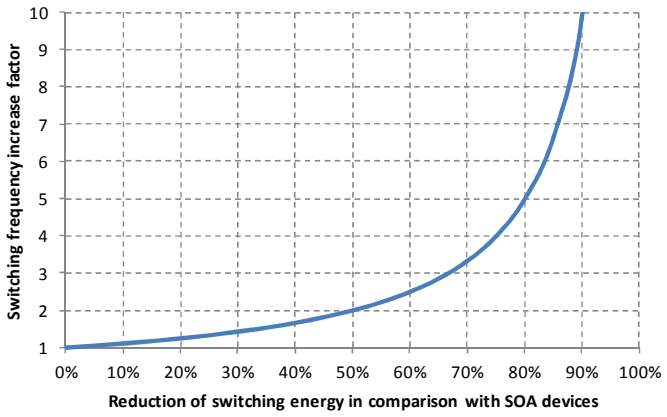

Figure 11: Reduction of switching energy against SOA power device and achievable switching frequency factor considering same overall level of losses.

Concerning the PV system, we propose in a first step to increase the operation frequency from currently 16 to about 48 kHz under the assumption that the overall switching losses remain the same. The driving circuitry will need to be adapted to this high switching speed in order to guarantee reliable operation. Last but not least, the use of new materials for isolation interfaces in the board, inductors and capacitors will be investigated aiming to prevent possible damage from voltage transients and to ensure the required levels of lifetime. The GaN-on-Si devices as proposed within the scope of this project offer the unique combination of high efficiency, high frequency capability and attractive cost-perspective which is able to address the above cited development challenges in PV systems. Capable of

higher switching frequencies, GaN devices will open the way to a significant reduction in size of the magnetic components and finally in massive cost savings not only of the magnetic component itself but also on the enclosure making 30% of the total bill of materials.

Higher switching frequencies are also an advantage for battery chargers and DCDC converters in electric vehicles resulting in more compact systems. Both automotive and PV systems will benefit from higher junction temperature operation (beyond actual levels of 175°C) and better heat spreading (beyond 200W/cm²), that will be also investigated within the scope of this project. This will enable higher device loading and chip area savings. Also the cooling requirements will decrease. This is interesting for PV applications, but much more for automotive applications where water cooling systems might be replaced by cheaper natural or forced air cooling in some cases.

5.4 Summary of the expected results

Table 1 below summarizes in a numerical form some of the major targets of the E²COGaN project on device, module and end application level. At the device level, several research papers exist that show the potential of GaN-based HEMT beyond the specifications set forth in Table 1. E.g. researchers at the Ferdinand Braun Institute of Berlin (O. Hilt et al., ISPSD2011, pp239-242) have reported E-mode device performance of V_{bd} ~1000V, Ron =0.63 mΩ.cm^2, Vth=1.1V, with a gate overdrive of 4V. The off-state leakage is low (~400 nA/mm at 600V). However, the devices were processed on 3" SiC substrates, and with a Au-containing metal stack. The authors use a carbon-doped buffer for reduced buffer leakage, which increases the dynamic Ron. A critical review of the literature data reveals that good device results are obtained on small wafer sizes (3" or 4"), mostly on SiC or sapphire substrates, and with a Au-containing metal stack (III-V labs) with no adequate reliability analysis. Achieving similar performance and improved reliability of GaN power devices on larger area wafers (6" and 8") in a low-cost CMOS compatible flow clearly brings the proposed work in this project beyond the state of the art; it also gives a clear message that GaN-on-Si can be scaled up to larger area wafers without jeopardizing device performance. Hence, meeting all the device parameters together on large wafer size Au-free processing is a major challenge, and has not been demonstrated before. On the module level, it has to be noted that currently there are no GaN modules available on the market or in publications. Only discrete devices are currently available. In principle, modules with about 10 nH computation path inductance are possible today, but it is not available in GaN. As for power density, the most modern power systems are with SiC devices and have a power density ranging between 80 and 100 kW/l. This is then also the target for the E²COGaN consortium since there is currently no information available from the market side. The only information that is available is for discrete GaN devices for low power systems.

GAN POWER DEVICE LEVEL			**State-of-the-art**	
Parameter	**Minimum requirement**	**Target specification**	**EPC**	**Transphorm[1]**
Operating voltage	600 V	600 V + exploration to higher voltages up to 1.5 kV	200 V	600 V
Threshold voltage V_T / enhancement mode (normally-off)	+ 1.0 V	+ 1.5 V (ideally above 2.5V for unipolar gate operation)	1.4 V	1.8 V (In cascode with LV Si MOSFET)

Negative gate voltage swing V_{GMIN}	V_T – 10 V	V_T – 10 V	-5 V	-10 V
Positive gate voltage swing V_{GMAX}	V_T + 3 V	V_T + 5 V	V_T + 4.5V	V_T + 10 V
Current rating	1 A to 20A	10 A to 100A	12 A	12 A (@ 100℃)
Specific on-resistance FOM R_{ON}*A	2 mΩ.cm^2 @ 600V	1 mΩ.cm^2 @ 600V	Ron = 25 mΩ	Ron = 150 mΩ (25℃)
Switching FOM R_{ON}*Qgd	30% reduction compared to SOA Si MOSFETs @ 600 V	<10x SOA Si MOSFETs @ 600 V	87.5-	NA
Inductive load switching times (600V, 10A)	10ns	2ns	NA	NA
Maximum junction temperature under operation	150℃	250℃	125℃	175℃
Gate to drain leakage at 600 V	< 1 µA/mm	< 10 nA/mm	50 µA, 160 V	10 µA
Forward Voltage V_F	2.0V @ 10A	1.7V @ 10A	1.5 V	2.16 V
GAN POWER MODULE LEVEL			**State-of-the-art**	
Parameter	**Minimum requirement**	**Target specification**	**PV Single Phase**	
Switching frequency	100 kHz	500 kHz	16 KHz	
Commutation path inductance	15 nH	5 nH	40 nH	
Power Density	200 W/cm^2	300 W/cm^2	<100W/cm^2	
Max. Temperature	175℃	175℃	150℃	
GAN POWER DEVICE DEMONSTRATOR			**State-of-the-art**	
Parameter	**Minimum requirement**	**Target specification**		
Switching frequency	50 kHz (PV) 250 kHz	100-250 kHz (PV)	16 kHz (PV) 250 kHz (Automotive)	

	(Automotive)	500 kHz (Automotive)	
Power conversion efficiency (for grid interfacing)	98.5% (PV) 97% (Automotive)	99% (PV) 98% (Automotive)	98.5% (PV) 97% (Automotive)
System volume*	-25%	-50% (PV) -60% (Automotive)	200 W/l (PV)
System cost*	-20%	-50% (PV) -30% (Automotive)	0.5€/W (PV)
Reliability (MTBF)	10 years	20 years (PV)	Normal 5 years guarantee, extendable up to 15 years (PV)

* with respect to a conventional Si-based solution

[1] The data was reported for a D-mode HEMT grown on SiC.and in cascode with a Si MOSFET.

Table 1: E²COGaN's minimum requirements and target performance specifications on GaN power device, module and demonstrator level. The contractual application demonstrators consist of a solar inverter in PV and a battery charger in Automotive respectively.

6.1 Overall strategy and general description

The general scope of this project is to develop the next generation of energy efficient power electronics based on a scalable, cost-effective, high-performing and reliable GaN-on-Si device technology platform. This platform will provide discrete and integrated devices suitable for 600V and higher (up to 1.5kV) and to prove their benefits at application level in automotive (full electric vehicles) and solar converter applications.

The strategy of the E^{2}COGaN project is to map the complete GaN power electronics value chain from wafer suppliers, semiconductor manufacturers and module makers to selected end users in the automotive and solar industry, comprising large industrial enterprises, SMEs and academics and applied research institutes. Added value will be assured by the presence of a number of highly specialized partners, such as simulation software houses, tool makers and experts in advanced characterization methodologies. It is our belief that the project can only be successful if all parties along the value chain work together, such that the wafer substrates, device technology and assembly of the module and the system take into account the requirements of the end user (which also include form factor, weight etc). A full iteration at the demonstrator level is foreseen, so that the devices and substrates can be modified to meet the end-goals at application level.

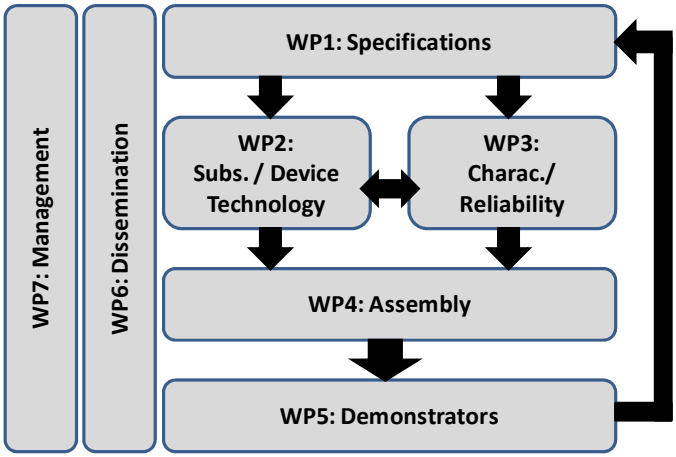

Figure 12: Schematic representation of the interrelationships between the different work packages.

To achieve the goals of E^{2}COGaN, the planned work will be structured into 7 different Work Packages (WPs). WP1 to WP5 represent the work flow through the value chain aiming to validate the potential of GaN power devices at each level starting at the application derived specifications to starting materials and technologies, through reliability to assembly and finally at the end application. WP6 formalizes the project's ambitions in dissemination and exploitation and WP7 is dedicated to the internal project management.

- WP1: Definition of Device and Application Specifications
- WP2: Substrate and Device Technology
- WP3: Characterisation, Reliability and Robustness
- WP4: Assembly and System Integration

- WP5: Application Demonstrators
- WP6: Dissemination and Exploitation
- WP7: Project Management

A graphical representation of the associated interdependencies of the different WPs is sketched in Figure 12.

Finally, Table 2 summarizes the involvement of the different partners in the above introduced the work packages highlighting major responsibilities with respect to the major goals of the E^2COGaN project.

The GANNT chart of the E^2COGaN project including major milestones and interdependencies is illustrated in Figure 13.

#	Shortname	N	WP1	WP2	WP3	WP4	WP5	WP6	WP7	Proposed Individual Contributions
1	ONsemi	BE	x	X	x	o	o	x	WPL	GaN HEMT and SBDs, 600V-1200V, 20A, d-mode -> e-mode, MISHEMT, mainly for automotive; characterization and reliability
2	NXP-NL	NL	x	X	X	x	x	x	x	GaN HEMT and SBDs, 600V -1200V, 20A, d-mode -> e-mode mainly for PV; failure analysis, physical charac., reliability
3	NXP-UK	UK	x	X	o	x	x		x	
4	NXP-B	BE	x	WPL	X	o	o	x	X	
5	ST-I	IT	x	X	X	X	X			8' devices processing, relaibility, micro-inverter demonstrator
6	Semikron	DE	x	o	o	X	o		x	GaN device module assembly for universal applications + characterization; gate driver solutions
7	CIRTEM	FR	x	o	o	X	X	x		main automotive demonstrator: EV battery charger
8	EPIGAN	BE	x	X	x	o	o	x	x	6" GaN-epi wafers 600 -> max , in-situ SiN, lower sheet resistivity (high Al content)
9	CISC	AT		o		o	X	x		system level simulation for GaN
10	NANO	SK		x	X	X		x	x	Multipulse UIS reliability testing and device recovery characterization at high temperatures
11	EADS	FR	x	o	X	X	x	x		aeronautics feasibility study (radiation, HT, failure mechanisms, reliability)
12	MC2 TECHNOLOGIES	FR		o	X			x		advanced pulsed characterization up to 1200V including hardware development
13	IUNET	IT		o	WPL			x	X	device failure analysis (trapping, dynamic RON, breakdown,..)
14	KDEE	DE	X	o	o	x	WPL	x	X	responsible for PV inverter demonstrator (3.5kW) including gate driver (discrete), PV specs
15	CEA LETI	FR	x	X	o	o	o	x		8" processing, 10->100AGaN HEMTs, assembly , drivers for GaN devices
16	FHG	DE	x	X	o	WPL	x	x	X	high temperature GaN module; high temperature gate driver (250°C); correlation crystal defects and electrical characteristics
17	STUBA	SK		x	X			x		TCAD and characterization
18	UNIVBRIS	UK		o	X	x		WPL	X	thermal and stress behaviour of GaN devices and modules
19	SNPS	CH		x	x	x		x	x	device and mixed mode modeling
20	BIT	DE	x	x			X			2nd automotive demonstrator: DC/DC converter
21	SE	FR	WPL	o	o	o	x	o	x	specs for industrial GaN applications, reliability, inverter circuit
22	AZZURRO	DE	o	X	o					6" and 8" GaN-epi wafers 600-1200V, multi-wafer tool epitaxy
23	BOSCH	DE	x	o		X	x		x	Assembly and packaging
24	TU/e	NL		o			X	x	x	transformer-less switch configurations
25	AUDI	DE	X	o			x			Automotive Specifications and final validation automotive demonstrator

Table 2: Overview of partners' individual contributions and their commitment in the different work packages [legend: WPL = Work Package Leader, X/x = major/minor contribution, o = observer status].

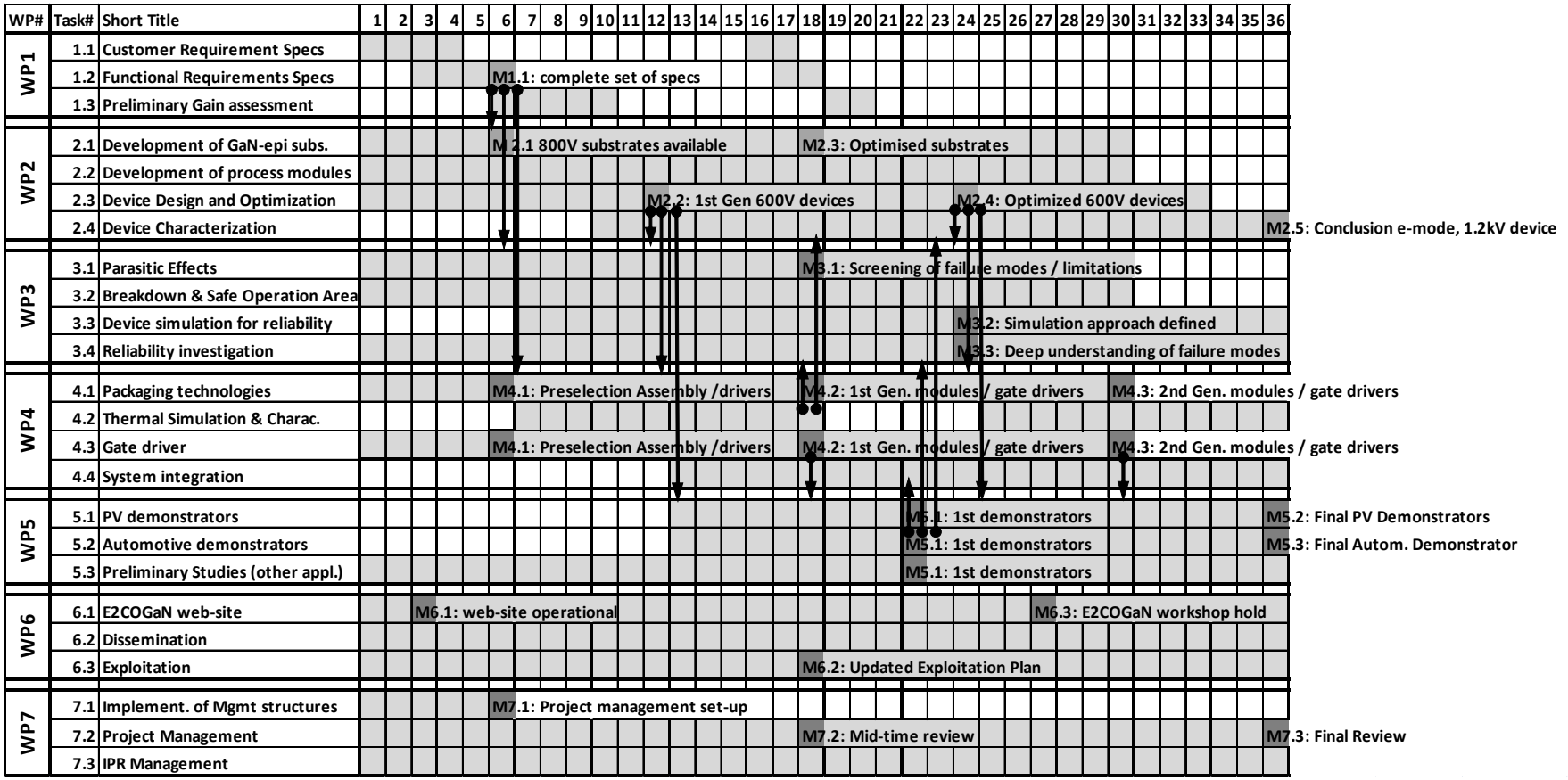

Figure 13: GANNT chart of the E²COGaN project including milestones and major interdependencies.

6.2 Work package description

Work package number	**1**
Work package title	**Definition of device and application specifications**
Work package leader	**SE**

Partner	**ON-semi**	**NXP-NL**	**NXP-UK**	**NXP-B**	**ST-I**	**Semi-kron**	**CIRTEM**	**EPIGAN**	**CISC**
Nat.	BE	NL	UK	BE	IT	DE	FR	BE	AT
PM	**7**	**4**	**4**	**4**	**8**	**1**	**2.5**	**1**	

Partner	**NANO**	**EADS**	**MC2**	**IUNET**	**KDEE**	**CEA-LETI**	**FHG**			**STUBA**
							IMS	**IZM**	**IISB**	
Nat.	SK	FR	FR	IT	DE	FR	DE			SK
PM		**2**			**4**	**1.5**	**1.8**	**2**		

Partner	**UNIVBRIS**	**SNPS**	**BIT**	**SE**	**Azzurro**	**BOSCH**	**TU/e**	**AUDI**	**TOTAL**
Nat.	UK	CH	IT	FR	DE	DE	NL	DE	
PM			**3**	**6**		**3**		5	**59.8**

Objectives of WP1

Based on the application requirements of the targeted demonstrators this work package will define the application key-specifications of the devices, modules specifications, from which are derived the epitaxy wafer, device, assembly and module and gate driver specifications that will serve as a guideline through the work packages and will enable to reach the project's goals. More precisely, it will identify the application / end-user's needs and the requirements in terms of cost, form factor and package, reliability and lifetime, operation temperature, voltage and current range, electrical performance, but also application constraints (such as related to the switching speed) and will translate them into specifications on epitaxy, process, device, module and gate driver level of WP1, 2 and 4, but also into reliability requirements for WP3. This task will require inputs from all industrial partners. WP1 comprises thus the following objectives:

- End-user application & demonstrator description
- GaN devices electrical parameters specifications adapted for end-user targeted demonstrators
- Epitaxy, process, device and module definition for GaN devices derived from end-user specification
- Assembly, packaging and gate driver specifications for GaN devices
- Estimation of the efficiency and/or overall passives elements (inductances, heatsink) reduction brought by the use of the specified GaN devices

Description of WP1

Task 1.1: Customer Requirement Specifications for Main Demonstrators

This task will draft the customer requirements for the application demonstrators of WP5. Each demonstrator specification will contain:

- Application overview: A general overview of system approaches for the selected target applications (photovoltaic, automotive, aeronautic, power inverters for industrial applications) will be presented. Key requirements (such as switching frequency) and constraints will also be discussed in order to identify development targets and potential gains. Afterwards, an outline of power conversion stages will be presented, with the objective of enabling the later selection of key device properties.
- Application-derived set of required key device specifications. In this task, the owners of the final demonstrators define the key device parameters based on the previous investigation of application. Key parameters to be defined are blocking voltage levels, breakdown profile, gate control levels (threshold, breakdown), leakage at gate and drain, specific chip resistance (and thus current ratings), maximum junction temperature, gate-drain charge. In addition to these, requirements regarding device reliability/testing will also be specified: required lifetime, mission profile (with thermal and loading stress levels), hardness against cosmic radiation (and advised voltage de-rating considering SEE), surge current withstand capability, voltage overshoot limits, requirements on robustness and finally validation tests of ECU (Electric Control Unit) and subcomponents. This part will also include an indication of key device parameters of Si or SiC devices used or suitable for these applications to have a representative comparison with the state of the art.
- Application-derived Assembly and Packaging key specifications. This part will define the requirements on the packaging in terms of power density, maximal inductance of commutation path, parasitic capacitances, thermal resistances (junction to case, case to sink), mounting instructions, possible high temperature environmental conditions (e.g. >200°C), thermal cycles (number and amplitude and relation to expected lifetime), maximal junction temperature on the packaging, assessment of EMI, achievable switching speed and frequency for every targeted assembled device/module.

	NXP-BE	NXP-NL	NXP-UK	ON-Semi	STMicro-I	Semikron	CIRTEM	EpiGaN	EADS	KDEE	FHG	BIT	SE	BOSCH	AUDI	CEA-LETI
MM		2	2		4	0.5	2.5		1	2.5		1.5	2.5	2	3	
Task 1.1: Customer requirement specifications for main demonstrators																
Application overview					X					X			X	X	X	
Application-derived set of required key device specifications					X	X	X		X	X		X	X	X	X	
Application-derived assembly and packaging key specifications		X	X		X	X	X			X			X	X	X	

Task 1.2: Functional Requirement Specifications in terms of GaN Power Epitaxy, Devices and Assembly

The technology providers of WP2 and WP4 will translate the customer requirement specifications into realistic, but challenging technology specification to answer on the required

key device and module parameters in close communication with the demonstrator owners of WP5. The specifications will then be translated into key technology choices that will drive the developments of WP2 and WP4.

- Epitaxy and Device specifications: Substrate provider and device manufacturer will translate the key requirements into epitaxy, architecture, layout, process and module choices enabling the implementation of the GaN power devices taking into account also the requirements from WP3 (in terms of robustness requirements, e.g. via smart epitaxy and layout choices) and WP4 (in terms of assembly requirements, e.g. via the adequate layout and metallization choices).

- Assembly, Packaging and Gate Driver Requirements: As a function of the customer requirement specification, but also of the device layout and processing constraints of WP2 the best suited packaging, assembly and gate driver approaches will be defined to be implemented in WP4. Special attention is paid to the reduction of circuit parasitics, capability of high switching speed with low level of oscillations, low values of thermal resistance, stability and finally competitive costs.

	NXP-BE	NXP-NL	NXP-UK	ON-Semi	STMicro-I	Semikron	CIRTEM	EpiGaN	EADS	KDEE	FHG	BIT	SE	BOSCH	AUDI	CEA-LETI
MM	4	2	2	7	2	0.25		1		0.5	3.8		0.5			1.5
Task 1.2: Functional requirement specifications in terms of GaN power epitaxy, devices and assembly																
Epitaxy and device specifications	X	X	X	X				X					X			X
Assembly, packaging and gate driver requirements	X	X	X	X	X	X				X	X		X			X

Task 1.3: Feedback into application specifications and preliminary gain assessment

The final task in WP1 will close the preliminary specification cycle by providing to the end-users and demonstrator developers the feedback from device and module manufactures regarding achievable goals. Such information will be translated into a first realistic gain assessment at system level in terms of increase in switching frequency and (tolerable) junction temperature, along with expected levels of conversion efficiency. Preliminary information regarding module footprint and device packaging approaches will also be provided in order to guide the preparations for the detailed design activities in WP5.

	NXP-BE	NXP-NL	NXP-UK	ON-Semi	STMicro-I	Semikron	CIRTEM	EpiGaN	EADS	KDEE	FHG	BIT	SE	BOSCH	AUDI	CEA-LETI
MM					2	0.25			1	1		1.5	3	1	2	
Task 1.3: Feedback into application specifications and preliminary gain assessment																
					X	X			X	X		X	X	X	X	

Risks and Mitigation of WP1

Specs for the different targeted applications might differ strong due to different application needs in terms. Mitigated through specific application focus per GaN power device supplier.

#	Deliverable	Owner	Due
D1.1.1	Customer Specification for PV inverter (4.5kW), Battery charger (3,5kW), PV microinverter (0.2kW) and industrial & power inverters	**SE,** BIT, CIRTEM, EADS, KDEE, ST-I, Semikron	T0+4

	verification: report with application description, customer requirements		
D1.2.1	Functional Requirement Specifications for main demonstrators verification: report with epitaxy, device, assembly and gate driver specifications	**ONsemi,** all partners WP1	T0+6
D1.2.2	Review of Functional Requirement Specifications for main demonstrators verification: updated report with epitaxy, device, assembly and gate driver specifications	**ST-I,** all partners WP1	T0+18
D1.3.1	Preliminary Report on Expected Gains on Application Level verification: report indicating expected gains (efficiency, size,..) of main demonstrators	**KDEE,** CIRTEM, ST-I, BIT, SE	T0+10

#	**Milestone**	**Owner**	**Due**
M1.1	Application-driven functional requirement specs for epi, device and module Verification: Report distributed to all WPs	**ONsemi**	T0+6
M1.2	Review of functional requirement specs Verification: Revised version of report distributed	**ST-I**	T0+18

GANNT

WP1 - Definition of device and application specifications — MM

	M4	M6	M9	M12	M15	M18	M21	M24	M27	M30	M33	M36	15
Task 1.1: Customer Requirement Specifications for Main Demonstrators	D.1.1.1	M1.1											

	M3	M6	M9	M12	M15	M18	M21	M24	M27	M30	M33	M36	40.5
Task 1.2: Functional Requirement Specifications in terms of GaN Power Epitaxy, Devices and Assembly		D.1.2.1				D.1.2.2 M1.2							

	M3	M6	M10	M12	M15	M18	M21	M24	M27	36	M33	M36	10
Task 1.3: Feedback into application specifications and preliminary gain assessment			D.1.3.1										

Work package number	**2**
Work package title	**Substrate and Device Technology**
Work package leader	**NXP-B**

Partner	**ON-semi**	**NXP-NL**	**NXP-UK**	**NXP-B**	**ST-I**	**Semi-kron**	**CIRTEM**	**EPIGAN**	**CISC**
Nat.	BE	NL	UK	BE	IT	DE	FR	BE	AT
PM	**231**	**91**	**61**	**55**	**36**			**50**	

Partner	**NANO**	**EADS**	**MC2**	**IUNET**	**KDEE**	**CEA-LETI**	**FHG**			**STUBA**
							IMS	**IZM**	**IISB**	
Nat.	SK	FR	FR	IT	DE	FR	DE			SK
PM	**2**					**43.5**			**41**	**12**

Partner	**UNIVBRIS**	**SNPS**	**BIT**	**SE**	**Azzurro**	**BOSCH**	**TU/e**	**AUDI**	**TOTAL**
Nat.	UK	CH	IT	FR	DE	DE	NL	DE	
PM	**0.5**	**2.5**	**2**		**108**				**735.5**

Objectives of WP2

Because of the close interdependency between GaN epitaxy substrate and GaN power device, substrate and device technology will be investigated, implemented and optimized *in one single* work package. Accordingly, the target of this work package is the engineering and optimisation of GaN-on-Si epitaxy substrates grown by MOCVD and the layout, process integration and technology of GaN power devices (HEMTs and Schottky diodes) implemented on these epitaxy substrates aiming to meet the specifications set forth in WP1, both at device level (including reliability requirements as investigated in WP3), assembly level (WP4) as well as at application level (WP5). The objective of WP2 is twofold :

- Availability of GaN-on-Si wafers from wafer vendors, meeting the specifications in terms of :
  - High voltage handling capability (800V first pass, 1.5 kV second pass for 600V and 1.2kV applications respectively)
  - Very low sheet resistance (below 250 Ω/square) to meet the Ron specification
  - Large, industry-relevant wafer sizes (6 inch, 8 inch)
  - Advanced surface passivations (in-situ and ex-situ), SiN capping versus other types of capping
  - New strain management and growth concepts for different 200mm substrates and for the growth on lower substrate thicknesses according to SEMI-Standards
  - Different Epi-Designs and fundamental material growth for new e-mode HEMTs with threshold voltage >1V

- Availability of HEMT power switches and Schottky rectifiers for further use in the reliability investigations (WP 3), in the assembly into modules (WP4) and finally in the project's main demonstrators of WP:
  - Voltage rating 600V (default), extension to1.2 kV
  - Current rating: several Amps up to 50A
  - Ron <2mΩ.cm^2 for 600V rating

- Bare die or standard package
- Theoretical and experimental exploration of several E-HEMT mode concepts, both from device design as from epi layer design
- Processed with a Au-free Si cleanroom compatible metallisation process
- Basic DC and AC characterisation, up to 300°C

Description of WP2

Task 2.1: Development of HV GaN-on-Si Epitaxy Substrates [Azzurro]

The GaN-on-Si layers must be crack-free and at a cost-competitive price, on both 6 inch and 8 inch. Silicon wafer thickness (625µm@150mm, 725µm@200mm) and wafer bow (<50µm) and warpage must be within the tolerance of standard CMOS processing equipments. Different research targets will be pursued :

(1) Investigation of different material combinations and layer thicknesses in buffer layers for defect reduction with appropriate strain management for flat 6 and 8 inch wafers after MOVPE withstanding 800V (1500V) with vertical leakage current of <1µA/<100nA, development of high Al concentration hetero-junction structures to reduce the sheet resistance below 250 Ω/square, to reduce specific on-resistance with FOM of R_{ON}*A< 2 mΩ.cm^2 @ 600V.

(2) Fundamental investigation of extended defect types introduced by buffer, epitaxy or device technology (edge and screw type dislocations, stacking faults, grain boundaries (tilt and twist), particles and other 3D defects), their densities and influence on the device performance and degradation mechanism is performed to fulfil device functionality and lifetime. Tilt and twist parameters are investigated for improved buffer crystal quality of epitaxially grown GaN layer on Silicon substrates and their influence on device performance and lifetime. Targets for the optimisation of wafer quality are low tilt (XRD-002 < 240arcsec) and twist (XRD-102 < 400arcsec) parameters to close the gap to GaN-on-Sapphire material quality. New buffer layer growth and designs are developed for basic defect reduction in HEMT-device layer from TDD = 8x10^8 cm^{-2} down to 4x10^8 cm^{-2} and 2x10^8 cm^{-2}.

(3) Study of the use of in-situ SiN capping layers to reduce surface states and hence to better surface passivation. Impact of different capping layers (GaN, SiN, …) on device reliability (in collaboration with WP3). Use of in-situ SiN to reduce possible cross-contamination in a CMOS fab. Systematic study of HEMT-Epilayer and capping on dynamic Ron behaviour and research for improved epitaxial layer for higher frequency operation up to 200kHz@600V with pulses down to 1µsec is necessary.

(4) Improved epitaxial designs will be studied to lower the forward voltage to V_f<2.0/1.7V of diodes;

(5) Research on new (MIS)-HEMT/Diode designs with extending the blocking voltage capability up to 1.2 kV, on both 6 inch and 8 inch wafers, on multi-wafer reactors;

(6) For the exploration of dedicated buffer structures targeting up to 1.5kV in-depth physical characterisation of the crystal quality and surface morphology of the layers will be done through X-Ray Diffraction (XRD), High Resolution X-Ray Diffraction (HRXRD), Photoluminescence (PL), Cathodo-Luminescence (CL), Electron Beam Induced Current (EBIC), high resolution Energy-Dispersive X-ray Spectroscopy (EDS), Atomic Force Microscopy (AFM), X-ray topography (XRT), Transmission Electron Microscopy (TEM), defect etching, and the results will be correlated with the device performance (Task 2.2).

	NXP-BE	NXP-NL	NXP-UK	ON-Semi	STMicro-I	EpiGaN	AZZURRO	CEA-LETI	STUBA	NanoDesign	UniBristol	Synopsys	FHG-IISB	Bitron
MM	0	0	0	0	0	50	96	6	0	0	0	0	41	0
Task 2.1: GaN-on-Si based Epi-wafer														
Improved Ron and dynamic Ron						X	X							
Buffer engineering for 1.5 kV						X	X							
GaN-on-Si on 8 inch substrates, 1.5 kV							X							
e-mode Epi-wafer and concepts							X							
Batch reactors--cost optimisation and competitiveness						X	X							
In-situ surface passivation						X		X						
Physical characterisation						X	X	X					X	

Task 2.2: Development of process modules for an Au-free Si CMOS compatible device process [CEA-LETI]

Development of the required process modules using a standard Si CMOS line equipment set, to target high volume production with Si-process-equivalent cost structure. The modules that need to be developed and optimised are :

(1) Isolation module, using either mesa etching or implantation; target is to have the isolation leakage current <100nA/mm at the rated voltage.
(2) Ohmic contact module using an Al-based metalisation, target is to reach <1Ω.mm.
(3) Schottky contact, with low leakage current (<1 µA/mm) and V_F <2V at 10A.
(4) Gate module for MISHEMTs, optimum gate dielectric stack using high-k insulators deposited with ALD, with no hysteresis and meeting insulator reliability specifications (especially at high temperatures, i.e. > 150 ^{o}C).
(5) Surface passivation, required to meet the current collapse specifications (less than 10% current collapse at 1 µs).
(6) high voltage backend process ; exploration of a high voltage backend process allowing for bonding on active and high temperature operation, using suitable monitoring structures (Q_{bd} and TDDB alike), along with a methodology to define the lifetime of the back-end process using accelerated testing methods.
(7) E-mode process: several approaches will be pursued from a device and process perspective, in combination with novel substrate layer design (see Task 2.1). Action on AlGaN layer to suppress 2DEG electrons gas under gate. Explore the possibility of normally-off devices based on MOSHEMTs .

This task will require a close loop between the wafer suppliers, the device manufacturers and academic institutes.

	NXP-BE	NXP-NL	NXP-UK	ON-Semi	STMicro-I	EpiGaN	AZZURRO	CEA-LETI	STUBA	NanoDesign	UniBristol	Synopsys	FHG-IISB	Bitron
MM	0	11	48	89	16	0	0	13,5	0	0	0	0	0	0
Task 2.2: Process Module Development														
Isolation module			X	X	X									
Ohmic contact			X	X	X			X						
Schottky contact			X	X	X									
Gate module for MISHEMTs		X		X										
Surface passivation				X				X						
High voltage backend for bonding on active				X										
E-mode device modules					X									

Task 2.3: Device design and optimization [ONsemi]

The pre-set device target specifications are 600V—1.2kV, up to 50A rating for both Schottky rectifiers as well as switching devices (HEMTs). In order to assure economic viability of the GaN power devices versus incumbent technologies, a competitive specific Ron of the HEMTs from 2 down to 1 $m\Omega.cm^2$ at 600V is targeted, including bondpad area (often omitted in R&D publications). Process and layout optimisation will be performed to achieve lowest on-resistance and gate charge, and best possible suppression of reliability and stability issues such as dynamic Ron, trapping phenomena or parameter drift as investigated in WP3. Special attention is paid to the E-field engineering near the gate to increase breakdown and device robustness via optimization of field plates using a full loop from theoretical investigations by TCAD simulations up to experimental verification through dedicated test structures on chips. The project team will start with D-mode (Schottky based and MIS based) HEMTs first, and will evaluate different E-mode concepts and their corresponding performance trade-offs in a second phase. TCAD simulations for E-mode will allow to select the most promising epitaxy, layout and process options (barrier recess, choice of gate dielectrics and charge balance, impact of E-mode channel length on total Ron, etc) in terms of manufacturability and reachable threshold voltage. For cascode solutions, mixed mode simulations will be used to determine the optimum choice of LV Si MOSFET to be co-packaged with the HV GaN HEMT (in terms of Ron, gate charge, leakage current etc.).

Another task consists in the definition and implementation of dedicated test structures to extract physical properties of buffer and interface properties, to be used to calibrate parameters of TCAD electro-physical models. This task will be a close collaboration between the wafer suppliers, the device manufacturers and academic institutes.

	NXP-BE	NXP-NL	NXP-UK	ON-Semi	STMicro-I	EpiGaN	AZZURRO	CEA-LETI	STUBA	NanoDesign	UniBristol	Synopsys	FHG-IISB	Bitron
MM	0	60	13	113	14	0	12	12	6	0	0	2,5	0	0
Task 2.3: Device design and optimisation														
TCAD simulation for testchip inputs		X		X	X		X	X				X		
E-mode TCAD concept evaluation					X		X		X			X		
E-mode through cascode design : mixed mode simulations				X					X					
Processing 600V rated HEMTs			X	X	X			X						
Processing 1.2kV rated HEMTs			X	X				X						

Task 2.4: Device characterization [NXP-B]

This task deals with the DC and AC characterisation of the devices (HEMTs and Schottky diodes) fabricated in Task 2.3. Important parameters are Ron as a function of current and temperature, Vth, Ioff, Igate, Vbd, gate charge extraction, Crss, Ciss, Coss, Vforward. Special focus is put on the evaluation of different device designs (e.g. field plate layouts for leakage, breakdown control, metallisation schemes, etc.). Statistical data collection will be done through automatic wafer mappings to determine probe yield. The DC and AC characterization will be performed from 40°C up to 300°C giving thus valuable input for device operation at extreme temperature conditions. Assembly in standard packages for dedicated testing (SO8FL, QFN, TO247, etc.) will be also part of this task. Another aspect is the investigation of different substrate connections under switching conditions (floating substrate versus grounded substrate) for direct feedback on the epitaxy choices and constraints of task 2.1.

	NXP-BE	NXP-NL	NXP-UK	ON-Semi	STMicro-I	EpiGaN	AZZURRO	CEA-LETI	STUBA	NanoDesign	UniBristol	Synopsys	FHG-IISB	Bitron
MM	55	20	0	37	6	0	0	12	6	2	0,5	0	0	1
Task 2.4: Device Characterisation														
DC characterisation	X	X		X	X			X	X	X	X			X
AC characterisation	X	X		X				X	X	X				
Floating substrate versus grounded substrate under switching		X		X										
Statistical data collection/yield				X										

Risks and Mitigation of WP2

- Substrates do not meet target specs for voltage rating, mechanical parameters etc. Mitigated by having different wafer suppliers and research partners in the consortium.
- Devices/technology do not meet electrical specs. Mitigated by having different device suppliers in the consortium and having collaboration with academia.
- Wafer cost remains too high, not cost competitive with Si and/or SiC; mitigation through 8 inch multi-wafer batch reactors.
- None of the device manufacturers deliver on-time ; mitigation through external foundry.
- Voltage capability of (Al)GaN buffers limited because of process issues (cracking, ….) :

#	Deliverable	Owner	Due
2.1.1	Characterization report of 800V 6 and 8 inch substrates. Verification : R_{SH} mapping or hall-data, wafer bow and warp, physical characterization at EpiGaN and AZZURRO; breakdown capabilities through processing of isolation structures in ON and NXP.	**EpiGaN** AZZURRO FHG IISB	T0+09
2.1.2	Characterization report of 1500V 6 and 8 inch substrates. Verification : R_{SH} mapping or hall data, wafer bow and warp, physical characterization at EpiGaN and AZZURRO.	**AZZURRO** EpiGaN FHG IISB	T0+24
2.1.3	Characterization report 6 and 8 inch epi-wafers for e-mode devices Verification: Demonstration of e-mode operation through basic wafer processing and testing at NXP, ONSemi and LETI	**NXP** CEA LETI AZZURRO ONSEMI ST-I FHG IISB	T0+27
2.2.1	Report on Au-free GaN power device baseline Verification: list and description of integration modules, Si-clean-room compatibility	**ONSemi** NXP-UK CEA LETI ST-I	T0+18
2.3.1	TCAD report on E-mode Device design, exploration of different concepts in combination with new epi stacks Verification: conclusion on best approach based on theoretical and practical aspects	**STUBA** AZZURRO	T0+12
2.4.1	Full electrical characterisation report on 600V rated D-mode HEMTs and Schottky rectifiers, 2nd pass, with focus on improved Ron and dynamic Ron Verification: static and dynamic characteristics of switches and rectifiers meets electrical specifications. Both Schottky-based HEMTs as well as MISHEMTs are available.	**NXP** ONSemi ST-I	T0+27
2.4.2	Full electrical characterisation report on 1200V rated HEMTs and schottky rectifiers Verification : static and dynamic characteristics of switches and rectifiers meets electrical specifications. Both Schottky-based HEMTs as well as MISHEMTs are available	**ONSemi** CEA LETI NXP	T0+33
2.4.3	Full electrical characterisation report of true E-mode HEMTs Verification : static and dynamic characteristics of switches and rectifiers meets electrical specifications.	**CEA LETI** **NXP-B** STUBA ST-I	T0+36

#	Milestone	Owner	Due
M2.1	1st Generation 800V epi-substrates : Verification: Substrates available for GaN device integration	**AZZURRO**	T0+6
M2.2	1st Generation 600V power devices,D-mode: Verification: GaN devices available for WP3 and WP4	**NXP-UK**	T0+12
M2.3	Optimised 6" and 8" epi-wafers available (R_{SH} <250 Ω/sq): Verification: Substrates available for GaN device integration	**EPIGAN**	T0+18
M2.4	Optimized 600V power devices available, D-mode : Verification: GaN devices available for WP3 and WP4 (reduced Ron,...)	**ONsemi**	T0+24
M2.5	Final conclusion on advanced GaN devices: e-mode and 1.2kV devices Verification: Final report available including critical discussion with respect to future applications	**CEA LETI**	T0+36

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	M3	M6	M9	M12	M15	M18	M21	M24	M27	M30	M33	M36
Task 2.1 GaN-on-Si Epitaxy												
Characterisation report 800V ; 6 and 8 inch		M2.1	D2.1.1									
Characterisation report 1500V ; 6 and 8 inch								D2.1.2				
Characterisation report E-mode wafers									D2.1.3			
Task 2.2 Process modules for Au-free processing												
Au-free power device baseline						D2.2.1						
Task 2.3 Device Design and Optimisation												
TCAD report on E-mode device design, new epi stacks				D2.3.1								
Processing 600V HEMTs				M2.2				M2.4				
Processing 1200V HEMTs ; E-mode												M2.5
Task 2.4 Device Characterisation												
Characterisation report 600V D-mode HEMTs and Schottky rectifiers									D2.4.1			
Characterisation report 1200V D-mode HEMTs and Schottky rectifiers											D2.4.2	
Characterisation report true E-mode HEMTs												D2.4.3

Work package number	**3**
Work package title	**Characterization, Reliability & Robustness**
Work package leader	**IUNET**

Partner	**ON-semi**	**NXP-NL**	**NXP-UK**	**NXP-B**	**ST-I**	**Semi-kron**	**CIRTEM**	**EPIGAN**	**CISC**
Nat.	BE	NL	UK	BE	IT	DE	FR	BE	AT
PM	**61**	**52**		**10**	**64**			**2**	

Partner	**NANO**	**EADS**	**MC2**	**IUNET**	**KDEE**	**CEA-LETI**	**FHG**			**STUBA**
							IMS	**IZM**	**IISB**	
Nat.	SK	FR	FR	IT	DE	FR	DE			SK
PM	**36**	**20**	**23**	**87**						**74**

Partner	**UNIVBRIS**	**SNPS**	**BIT**	**SE**	**Azzurro**	**BOSCH**	**TU/e**	**AUDI**	**TOTAL**
Nat.	UK	CH	IT	FR	DE	DE	NL	DE	
PM	**23**	**10**							**462**

Objectives of WP3

The main objectives of this work package is to study GaN power device specific limitations in terms of parasitic, thermal and reliability issues, to establish the safe-operating-area and to provide valuable feedback to the device and substrate R&D activity of WP2 targeting a reliable, robust and parasitic-free GaN HEMT power technology. Via lifetime predictions valuable information will be provided to WP4 and WP5 enabling the conception of modules, gate drivers and finally the target applications. It has to be noted that the reliability assessment of WP3 is restricted to device-intrinsic aspects as studied on wafer level and in standard packages. Reliability and robustness aspects related to packaging and assembly activities within WP4 are directly studied in WP4.

More precisely, the identified objectives are:

- Understanding of parasitic phenomena in power GaN HEMTs and Schottky diodes (trapping, gate leakage, drain leakage) through advanced characterization and modeling and assessment of technological countermeasures
- Understanding of thermal limitations of power GaN HEMTs
- Understanding of breakdown phenomena and identification of the device Safe Operating Area (SOA)
- Development of electro-physical models for 2D / 3D simulations of GaN-based devices with special focus on parasitic phenomena and breakdown behavior
- Identification of device failure modes and mechanisms and recommendations towards their solution to be implemented in WP2 enabling the development of a robust and reliable GaN–based technology
- Lifetime prediction regarding their use in target applications

Description of WP3

Recent advances in the development of GaN Power High Electron Mobility Transistors (HEMTs) and in their processing using cost-scalable GaN-on-Si epitaxy substrates, will open the way to a wide range of applications in the power conversion field. Their superior performance in terms of bandwidth, low and attractive R_{DSON}-Q_{GATE} product, limited dependence on temperature of the threshold voltage and the channel resistance R_{DSON}, capability to operate at high junction temperatures and radiation hardness are expected to give a remarkable improvement in the energy conversion field. Moreover the optoelectronics market growth is pushing investment to increase wafer size, so it is mandatory to look at aspects related to eight inch CMOS front end compatibility. This being said, there still remain technological barriers to overcome in order to put GaN-based devices into practical use. Summarizing, these are the most critical issues to be solved in gaN HEMT devices:

- Availability of parasitic-free (i.e. trap-free) devices
- Reduction of the gate leakage current
- Understanding of hot electrons and breakdown phenomena
- Assessment and understanding the GaN-device behavior at high temperatures
- Availability of reliable and robust GaN-HEMTs enabling to boost applications in energy efficiency and compactness

To fill these gaps, a detailed activity of device characterization, parasitic phenomena investigation, in conjunction with 2D/3D device simulations and a detailed reliability investigation is largely required. To this aim an extensive device characterization and reliability investigation will be carried out addressing mainly the following points:

i) Evaluation of device operation at high temperatures (>200 ºC)
ii) Assessment of self-heating phenomena in GaN Power devices
iii) Characterization of trapping phenomena under realistic switching conditions
iv) Understanding of breakdown phenomena and identification of the Safe operating Area (SOA)
v) Reliability investigation and identification of failure modes and mechanisms
vi) Lifetime prediction for future applications

The above-mentioned activities will be carried in conjunction with combined electro/optical measurements and TCAD electro/thermo/mechanical simulations. This combined approach will allow an in-depth understanding of device behavior under high voltage conditions and identifying the device SOA. Long-term reliability assessment will also be carried out with the aim of lifetime prediction. Finally ESD, UIS and radiation sensitivity evaluation will also be investigated.

This project is composed by a large consortium and includes 3 foundries: NXP, ONsemi and ST-I. Large effort will be hence necessary in order to characterize large number of devices that will come out in parallel by three sources. For this reason in the task description, below reported, it will be noted that more than one partner is involved in each activity. This is to provide an adequate availability of characterization sites, required for the large device delivery expected from WP2. The access to different foundry devices will provide unique opportunities for this part of the project, to enable to distinguish between growth, fabrication and physics originating performance and reliability impacting factors, providing a unique opportunity for Europe for advancing this technology.

Task 3.1: Device characterization and parasitic effects evaluation (TL: UNIVBRIS)

The aim of this task is to accurately identify the main parasitic effect and the device performance in order to verify if the specifications required for the specific application of this project are achieved. Test structure design and testing methodologies will be defined in the initial part of this activity. Parasitic effects like gate leakage current, drain leakage current, charge trapping leading to current collapse and R_{DSON} transients, kink phenomena, will be studied in detail in order obtain a detailed characterization of all these problems. Thermal

characterization, heat transfer and novel techniques will be employed with the aim of fully understanding the device operation in the operating conditions. Electroluminescence and noise measurements will be employed with the aim of carefully identifying gate leakage issues. Specific Unclamped Inductive Switching (UIS) tests will be developed in order to characterize devices during real operating conditions. Finally, specific high voltage pulse set ups, up to 1000V will also be developed, enabling to study the HV device behaviour at switching speeds down to few ns. The role of each partner in Task 3.1 is reported below.

	IUNET	MC2	UNIVBRIS	NXP-B	NXP-NL	Onsemi	ST-I	STUBA	Nanodesign	SNPS	EADS	EPIGAN	TOT
MM	**23**	**10**	**11**	**0**	**22**	**20**	**10**	**24**	**18**	**0**	**0**	**1**	**139**
Task 3.1: Device Characterization and Parasitic effect evaluation - Task Leader UNIVBRIS													
Trapping Characterization (Pulsed, DLTS, transient, Dyn Rdson)	X	X			X	X		X	X			x	
High Temperature Characterization					X	X	X		X				
Electroluminescence	X		X										
Thermal characterization, heat transfer, novel techniques			X			X							
Noise Measurements	X							X					
Unclamped inductive switching (UIS)					X	X	X	X	X				
Development of specific probes and characterization procedures for high voltages.		X											
Development of HV Pulse setup (1000 V)		X											

Task 3.2: Breakdown and SOA Evaluation (TL: NXP-NL).

The basic physical mechanisms leading to breakdown will be deeply analysed using DC and pulsed electrical measurements performed at different ambient temperatures as a function of epitaxy, process and layout choices. OFF-state as well as ON-state breakdown will be studied in three terminal configurations, and correlated with the simulations of Task 3.3. Electroluminescence will also be employed in order to identify uniformity and specific localized breakdown sites within the devices active area. The aim of this activity will be the identification of the device Safe Operating Area (SOA). The role of each partner in Task 3.2 is reported below.

	IUNET	MC2	UNIVBRIS	NXP-B	NXP-NL	Onsemi	ST-I	STUBA	Nanodesign	SNPS	EADS	EPIGAN	TOT
MM	**20**	**6**	**0**	**6**	**16**	**15**	**18**	**0**	**0**	**0**	**0**	**0**	**81**
Task 3.2: Breakdown and SOA evaluation													
2- and 3- terminal DC Breakdown investigation	X	X		X	X	X	X						
OFF state breakdown	X	X		X	X	X	X						
ON state Breakdown (Pulsed) and Vs Temperature	X	X											
SOA definbition	X				X	X	X						

Task 3.3: Device Simulation for reliability investigation (TL: SNPS).

The device simulation of power GaN HEMTs still presents several challenges with respect to the device operation at high electric field/temperature, modelling of trapping and de-trapping phenomena and to the modelling of the degradation mechanisms. Models of high–field carrier transport and impact-ionization will be evaluated and developed. Furthermore TCAD simulators will be employed in order to study the trapping phenomena and reliability issues in power GaN devices with the aim of a predictive approach for the development of robust and reliable devices. Thermal and self-heating effects will also be simulated and linked to the experimental data from Task 3.1. Simulations methodologies that allow fast and robust simulations will be developed and implemented. The role of each partner in Task 3.3 is reported below.

	IUNET	MC2	UNIVBRIS	NXP-B	NXP-NL	Onsemi	ST-I	STUBA	Nanodesign	SNPS	EADS	EPIGAN	TOT
MM	22	0	5	0	0	0	16	24	0	10	0	0	77
Task 3.3: Device simulation TCAD													
TCAD simulation and the investigation of trapping	X						X	X		X			
Models of high –field hot carrier transport, impact ionization	X									X			
Distributed self-heating effects	X		X							X			
Electro/Thermo/mechanical simulations.	X		X							X			
investigation of influence of radiation on device properties										X			
SPICE based circuit simulators								X					

Task 3.4: Reliability investigation (TL: IUNET).

In this task the evaluation of the **short-term** and **long-term** stability of the electrical and physical characteristics of the power GaN HEMT devices developed in WP2 will be carried out. The definition of the lifetime tests, the failure criteria and the test conditions will be defined at the initial stage of this task. The main goal of this activity will be the identification of GaN device specific device parameter drifts and failure modes and mechanisms of power switching GaN HEMTs and their correlation with the different device substrates and gate topologies. The adoption of advanced failure analyses like Spectrally-Resolved Cathodoluminescence (SCL) in scanning electron microscope (SEM), micro-photoluminescence (µPL), UV and VIS micro-Raman spectroscopy (µRS), and FIB/TEM investigation will allow an in-depth understanding of the degradation physics. The Electro Static Discharge (ESD) and Unclamped Inductive Switching (UIS) robustness, and the impact of radiation exposure and the sensitivity to the Single Event Effects (SEE) will also be investigated. The severity of the different device instabilities will be assessed together with WP4 and WP5 for each targeted application in order to give consolidated recommendations for further device and epitaxy wafer optimisation in WP2. Furthermore, work will be dedicated to define lifetime suitable power GaN device criteria and applied to the GaN power devices of WP2. The role of each partner in Task 3.4 is reported below.

	IUNET	MC2	UNIVBRIS	NXP-B	NXP-NL	Onsemi	ST-I	STUBA	Nanodesign	SNPS	EADS	EPIGAN	TOT
MM	22	6	7	4	14	26	20	26	18	0	15	1	159
Task 3.4: Reliability investigation and Material Characterization													
Test Structure and test methodologies definition	X		X	X	X	X	X	X				x	
Thermal storage and accelerated testing,	X			X	X		X						
Wafer level short term reliability and identification of Failure modes and Mechanisms	X	X			X				X				
Characterization of **structure, strain and defects** (SCL, SEM, uPL, uRaman)			X					X					
Investigation of **degradation mechanisms (SCL, uPL,SuRaman, EM/EBIC/TEM)**			X					X	X				
long-term reliability study (HTRB, H3TRB, HTGB, etc)	X				X	X	X						
TDDB of MISHEMT structures + extrapolation models						X							
Reliability assessment of device in standard (simple) package.							X		X		X		
ESD sensitivity	X												
Radiation sensitivity and Single Event Effect	X										X		

Risks and Mitigation in WP3

WP3 is a characterization and simulation work package, consequently there are no intrinsic major risks that could hamper the success of this project, but the relevance of the outcome of this WP is of course dependent on the device and substrate quality as delivered from WP2.

From the characterization point of view, developing characterization set-ups capable of high currents, high voltages and/or fast switching is very challenging. At the same time, thermal management during measurements is extremely important and not trivial. Finally, the development of drift-diffusion and/or hydrodynamic 2D/3D devices simulation in GaN devices, is also quite challenging, due to the very complex nature of the GaN epitaxy and device structure.

Concerning the characterization hardware availability, the risk is mitigated by having with MC2 a key supplier on board allowing us to carry out measurements on equipment beyond the state-of-the-art.

Concerning the correctness and appropriateness of characterization methodologies and interpretation of the results risk mitigation is assured by having on board a broad consortium of leading European researchers in the field of characterization and simulation of GaN power devices.

In order to guarantee timely availability of first conclusions on parameter drift and failure modes, early characterization/simulation activity will be carried out on using faster available small R&D devices before validation on large and application-relevant devices once those are available.

	Deliverable	Owner	Due
D3.1.1	GaN Power Device behavior and limitations including breakdown data from Task 3.2 Verification: Report on device performances limitations (Ron, Leakage, Breakdown, trapping), thermal device aspects, high temperature operation, noise measurements, OFF state leakage current, Maximum Voltage/Current operating values	**UNIVBRIS,** IUNET, NXP-NL, NXP-B, ONsemi, ST-I, STUBA, MC2, NANO	T0+15
D3.1.2	Unclamped inductive switching (UIS) and HV Pulse Set-UP Verification: Report on operation of devices in unclamped inductive switching, operating at high Voltage-Current conditions, devices.	**MC2**, NXP-NL, ONsemi, NANO	T0+30
D3.2.1	GaN Power Device breakdown behavior and limitations (	common with D3.1.1)	T0+15
D3.2.2	SOA Definition Verification: Report on SOA as function of epitaxy, layout and process choices	**ST-I**, IUNET, MC2**,** NXP-NL, NXP_B, ONsemi,	T0+30
D3.3.1	TCAD and SPICE simulations including trapping and de-trapping effects, self heating and high field phenomena Verification. Comparison of experimental and simulated electrical characteristics of selected GaN devices	**SNPS**, ST-I, IUNET, STUBA,	T0+30
D3.3.2	TCAD Electro/Thermo/mechanical simulations and investigation of radiation effects Verification. TCAD simulations well describing the characterization measurements, radiation effects included in the simulators.	**SNPS**, IUNET, UNIVBRIS, IUNET	T0+36
D3.4.1	Definition of test structures for reliability investigation, methodologies, lifetime requirements for applications Verification: Diversity of designed test structures, dedicated test structures for reliability investigation, test methodology defined	**IUNET,** MC2**,** UNIVBRIS**,** , NXP-NL, NXP-B, ONsemi, ST-I, EADS	T0+06
D3.4.2	Identification and interpretation of stress-induced failure modes and mechanisms in Power devices including physical device and material investigations (SCL, uPL, Raman, EBIC/SEM/TEM) Verification: Report on main failure mechanisms and their origins with recommendation of device / epitaxy improvements	**IUNET,** MC2**,** UNIVBRIS**,** , NXP-NL, NXP-B, ONsemi, ST-I, STUBA, NANO	T0+18
D3.4.3	Final reliability and lifetime assessment of GaN Devices including UIS, ESD and Radiation sensitivity (SSE) Verification: Report on Estimation of device lifetime in operating conditions, ESD and radiation sensitivity evaluated.	**IUNET,** MC2**,** UNIVBRIS**,** , NXP-NL, NXP-B, ONsemi, ST-I, EADS, NANO	T0+36

	Milestone	Owner	Due
M3.1	Conclusions on screening of failure modes and thermal limitations in GaN Power devices	UNIVBRIS	T0+18

	Verification: Report available: list of failure modes and severity regarding application		
M3.2	Simulation approach for reliability investigation and lifetime predictions in GaN power device: Verification: TCAD approach for reliability investigation implemented	SNPS	T0+24
M3.3	Most relevant failure modes and device limitations understood and recommendation list for reliability improvement: Verification: Report available on failure modes, origins and possible solutions	IUNET	T0+24

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WP3 - Characterization, Reliability and Robustness

Task 3.1: Device Characterization and Parasitic effect evaluation - Task Leader UNIVBRIS	**M3**	**M6**	**M9**	**M12**	**M15**	**M18**	**M21**	**M24**	**M27**	**M30**	**M33**	**M36**
Trapping Characterization (Pulsed, DLTS, transient, Dyn Rdson), High Temperature, EL, Thermal, Noise					**D3.1.1**	**M3.1**						
Unclamped inductive switching (UIS), HV Pulse set-UP										**D3.1.2**		

Task 3.2: Breakdown and SOA evaluation - Task Leader NXP-NL	**M3**	**M6**	**M9**	**M12**	**M15**	**M18**	**M21**	**M24**	**M27**	**M30**	**M33**	**M36**
Breakdown investigation (ON, OFF)					**D3.2.1**							
SOA definition										**D3.2.2**		

Task 3.3: Device simulation TCAD - Task Leader SNPS	**M3**	**M6**	**M9**	**M12**	**M15**	**M18**	**M21**	**M24**	**M27**	**M30**	**M33**	**M36**
TCAD and SPICE simulation with investigation of trapping, high field and self heating effects								**M3.2**		**D3.3.1**		
Electro/Thermo/mechanical simulations and investigation of Radiation effects												**D3.3.2**

Task 3.4: Reliability investigation and Material Characterization - - Task Leader IUNET	**M3**	**M6**	**M9**	**M12**	**M15**	**M18**	**M21**	**M24**	**M27**	**M30**	**M33**	**M36**
Test Structure and test Methodology Definition		**D3.4.1**										
Identification and interpretation of stress-induced failure modes and mechanisms in Power devices including physical device and material investigations (SCL, uPL, Raman, EBIC/SEM/TEM)						**D3.4.2**		**M3.3**				
Long-term reliability study (HTRB, H3TRB, HTGB, etc), ESD, Radiation sensitivity												**D3.4.3**

Work package number	**4**
Work package title	**Assembly and System Integration**
Work package leader	**FhG-IZM**

Partner	**ON-semi**	**NXP-NL**	**NXP-UK**	**NXP-B**	**ST-I**	**Semi-kron**	**CIRTEM**	**EPIGAN**	**CISC**
Nat.	BE	NL	UK	BE	IT	DE	FR	BE	AT
PM		**2**	**2**		**36**	**72**	**22.6**		

Partner	**NANO**	**EADS**	**MC2**	**IUNET**	**KDEE**	**CEA-LETI**	**FHG**			**STUBA**
							IMS	**IZM**	**IISB**	
Nat.	SK	FR	FR	IT	DE	FR	DE			SK
PM	**30**	**22**			**5.5**		**55.6**	**91.14**		

Partner	**UNIVBRIS**	**SNPS**	**BIT**	**SE**	**Azzurro**	**BOSCH**	**TU/e**	**AUDI**	**TOTAL**
Nat.	UK	CH	IT	FR	DE	DE	NL	**DE**	
PM	**2**	**1**				**34**			**375.84**

Objectives of WP4

This work package explores and develops the packaging and assembly concepts of GaN power devices as well as for suitable gate drivers and monitoring circuits to provide integration concepts for intelligent power modules and systems.

In order to integrate GaN semiconductors in applications they need to be assembled and integrated in a working system. This enables testability (within WP4) and applicability (for WP 5). In order to make optimum use of the specific features of GaN the assembly and system integration technology have to be adapted as standard concepts would not allow high temperature and high frequency operation. More precisely, WP4 focuses on the following objectives:

- Standard packages of GaN devices for early use in WP5
- New technologies for assembly of GaN devices and for improved reliability and higher operation temperatures up to 250°C.
- Reliability and robustness of advanced packages and gate drivers for specific aeronautic requirements (>200°C)
- New technologies and constructions/designs with lower parasitic inductivities for faster switching of GaN-devices
- Application circuits for GaN devices
- Gate driver technology and monitoring circuits and integration for higher operating temperature
- Evaluation and benchmarking of retained solutions against Si and SiC based power modules
- Complete integration of GaN devices in Intelligent Power Modules and power systems

Description of WP4

Task 4.1 Packaging Technologies (Semikron, FhG-IZM, CIRTEM, BOSCH)

Assemblies will be used for the fabrication of reliability test vehicles and for implementation in the demonstrators in WP5. In the beginning of the project the packaging concepts and flow of materials will be prepared and shared with all partners.

Standard Assembly:

Semikron: Standard technologies will be used for the assembly of GaN devices (GaN transistors, diode or GaN transistor (normally-on) and MOSFET in cascode topology etc.) in power modules and systems in different circuit topologies. The standard assembly technology will be based on soldering or gluing and heavy wire bonding and will result in early demonstrators for immediate characterization when new devices are available.

Bosch: Evaluation of the process and robustness capabilities of several new thick wire bonding materials (Al-alloys and Cu) on standard assembly of GaN devices.

Flip-Chip:

FhG-IZM: For flip-chip mounting bumps will be deposited on wafer level (GaN), preferably Au/Sn or Cu/Sn pillar bumps or contact pads. The selection of bump composition will depend on the choice of substrate technology and the metal / passivation stacks of GaN devices. The substrate technology has to meet the interconnect constraints from the GaN devices (contact area and space), current capability, thermal as well as reliability requirements. AlN thin film substrates might be required if DAB or DCB cannot meet the fine line pattern. GaN devices are flip-chip bonded to the substrate by soldering of Au/Sn or Cu/Sn. Using appropriate bump composition, bonding temperature and time the solder could be transformed into an intermetallic compound in order to increase the remelting temperature of the solder joints. The backside of the flipped devices can be used for the attachment of a heat spreader, heat sinks or for double sided cooling.

CIRTEM: Design and implementation of a half bridge inverter assembly. This prototype will be tested in WP5 in addition to the automotive demonstrator.

Bosch: Application of the new Cu/Sn-diffusion solder paste developed in the BMBF public funded project HotPowCon as a high robust flip-chip joining technology for GaN lateral power devices. Processing the paste, reflow soldering with triggering the diffusion process and the integration of further passive components on module level lead to the identification of the technology capabilites and determination of the robustness within task 4.5.

Advanced Die Bonding

Semikron: A new low temperature sinter assembly technology will be applied to GaN devices in power modules and systems in different circuit topologies for high temperature operation (up to 200°C and above). They will result in demonstrators with backside sintering and frontside bonding. The sinter technology requires a noble metallization (Ag, Pd, Au). The sinter technology allows operation temperatures up to 200°C, a better thermal resistance and cooling of the power devices, higher power densities and higher available currents, smaller and low inductive packages, higher output power capability per litre (volume), lower cost per available ampere and last, but not least a higher power cycle capability (10…20 times higher as the international standard today), a higher reliability and lifetime.

Bosch: Interactions between printing process with stencil and screen with the chosen silver sintering flakes or pastes have to be identified and possibilities in printable structures for lateral chip design have to be described. Assuming a strong influence between chip-metallization and load capability of the sintered joint the description of requirements for the chip back-end process is essential for the maximum robustness in power cycling in the region of maximum operating $T_{junction}$ or passive temperature cycling with maximum temperature swing. The qualification of joint robustness with respect to the characteristics of chip-metallization will be performed.

CIRTEM: Design of dual substrate sandwich assembly for automotive demonstrator (battery charger of task 5.2) without wire bonding. The GaN devices will be assembled by soldering or sintering of backside and frontside. This assembly technology requires GaN devices with Ag or Au back side and front side metallization (Ag prefered) from WP2. This technology allows the cooling of the two faces of the device, improved reliability without sacrificing the layout.

Task 4.2 Thermal Simulation, Characterization and Reliability (FhG-IZM, EADS, NXP-NL, NXP-UK, Semikron, SNPS, UNIVBRIS, Bosch, NANO, CIRTEM)

Assemblies and test samples from Task 4.1 will be used in order to evaluate the solutions with respect to thermal, electrical and reliability characteristics. The common goal is to use the results as a base for technology and design optimisation with respect to the WP4 objectives (see above), to enable a benchmarking against other Si and SiC based solutions, to indicate key electrical parameters to WP5 and to do a reliability evaluation with respect to specific application needs.

Thermal Simulation & Characterization

FhG-IZM: Interconnect and system level thermal models will be generated in order to analyse main heat paths and identify design options and size limits of the assemblies. Sensitivity analyses will be done with the models in order to deduce main influence factors. Transient and Lock-In Infrared Thermal characterisation will be used to verify models and characterise interconnect and device properties (i.e. TLSP, Sinter silver).

UNIVBRIS: Die attached chip thermal performance will be assessed using Raman thermography to characterize and understand heat flow pathways through the die attaches, also limitation of interfaces related to the advanced mounting and packaging. Thermal simulations will be performed in conjunction with the experimental thermal characterization.

SNPS: Synopsys will compare simulations done in WP3 with characterization results and simulations of the thermal and mechanical behaviour of the devices performed in WP4. These evaluation results will be used to calibrate and to validate the device simulations in WP3.

Bosch: R_{th}/Z_{th}-measurements of the chosen assembly (single-sided or double sided cooling concepts) by electrical excitation of the power switch, simulation of the thermal characteristics on single switch samples and module level.

Thermo-mechanical simulations & characterization

FhG-IZM Based on the thermal models also thermo-mechanical models will be deduced for the Flip Chip Assembly of Task 4.1, which will be based on measurement of dedicated material properties for the high temperature regime. Results will be correlated to the results of reliability assessment in order to give guidelines for improved reliability.

Bosch: Thermo-mechanical simulation of the die attach assemblies derived from task 4.1

EADS : thermo-electro-mechanical simulations of packaging in high temperature environments representative of aeronautic constraints (up to 200°C) will be performed

Device characterization and reliability assessment on module and assembly level

FhG-IZM will perform passive temperature cycling and high temperature storage tests and detects the degradation of electrical parameters. The failure modes will be investigated by C-SAM (interface delamination), X-Ray (e.g. partly melting) and analysis of the modules in cross-sections.

Semikron will perform

a) complete static characterization of GaN devices in the assembled modules: V_{br}, (leakage currents), R_{on}, V_{th} (output and transfer characteristic) V_{br} and V_f (forward voltage).
b) complete dynamic characterization of GaN devices in the assembled modules:
   - switching behaviour (double pulse measurements) of transistor, determination of E_{on}, E_{off}, V_{cemax}, dI/dt, dU/dt, Q_{rr} and I_{rr} of the anti-parallel freewheeling diode (FWD) depending from R_g, current density, V_{dc}-link, temperature;
   - short circuit behaviour with different inductivities;
   - switching behaviour under parallel device operation for higher currents.
c) reliability tests like HTRB, H3TRB (85% humidity, 85°C, 80% of V_{br}), power cycle test under different conditions.

EADS will perform reliability tests for specific aeronautic requirements (>200°C temperature cycling). Failure mode and mechanisms will be determined by failure analysis. Gate driver reliability will be assessed for aeronautic specific requirements (>200°C) using previously developed gate driver. In addition electromagnetic compatibility studies (EMC – susceptibility and immunity issues) of dies in the package will be investigated.

NANO will perform the following analysis on samples provided by partners:
- AC/DC and pulse measurements
- Voltage stress test at room and elevated temperatures up to 500°C
- Pulse and multipulse UIS test
- Switching characteristics with 1 ns resolution
- Low frequency noise analysis
- Failure analysis based on combination of electrical characteristics and SEM/EDS and spectral cathodo-luminiscence measurements

Bosch: Active power cycling tests of GaN transistors on different kind of packaging level, additional passive temperature cycling and reliability testing in coordination with the other WP4 partners. Determination life-time curves and comparison of these curves with life-time data of vertical switch concepts. Adjustment with automotive requirements.

CIRTEM: Die attach and assembly related tests: shear test, passive power cycling. Static and dynamic electrical characterizations of assemblies.

Task 4.3 Electrical and gate driver implementation (FhG-IMS, CEA-LETI, Semikron, ST-I)

Semikron: Gate driver for inverter

a) Development of application circuits for GaN normally-on devices for power applications, e.g. cascode topologies with LV MOSFETs in series
b) Development of gate driver circuits (ICs) for normally-on GaN devices with integrated level shifter and isolation for 600V and 1200V respectively [adaptation of isolation voltage, gate drive voltage, frequency, interlock time, short pulse suppression, gate driver stages and monitoring functions (short circuit, temperature etc.)]. The integration of the gate driver IC is based on a high voltage SOI-CMOS process and is fully functional up to 200°C (standard today max. 150°C).

ST-I: Gate driver for micro-inverter demonstrator

The Gate driver for the micro-inverter demonstrator of task 5.1 will be specified and realized to operate with a GaN switch in a multi-platform technology. GaN HEMT will operate with very high switching speed: this implies a gate drive able to emphasize GaN peculiarities minimizing parasitic effects coming from board, package and chip layout. Main requisites are: minimize pull down resistance in order to improve noise immunity down to 0.5Ω. Accurate gate drive supply voltage in order not to exceed maximum allowable gate voltage and avoiding unintentional turn-on due to the lower threshold voltage. Low gate drive loop impedance: driver must be placed as close as possible to HEMT. dV/dt immunity: since switching dV/dt will be close to 20-30 V/nsec, 50 V/nsec immunity is required.

FhG-IMS: High temperature gate driver for aeronautic requirement analysis (EADS). The aim of this task is to further analyze the GaN specific design constraints and the additional constraints resulting from the extended operating range capabilities of GaN power devices (e.g. higher operating temperatures, increased switching frequency). Based on this an optimized driver circuitry will be developed. The driver is a single gate driver featuring high temperature operation (250°C) and over temperature detection. Technology basis for the high temperature capable GaN gate driver will be a thin film SOI CMOS process. The thin silicon film (about 150nm) nearly eliminates the detrimental diode leakage currents at high temperatures and thus enables the chip operation up to 250°C. A high temperature metallization based on Tungsten guarantees excellent reliability with regard to electro-migration. The driver will be fabricated in the IMS CMOS fabrication line on 200 mm wafers. Within the project the GaN devices will be assembled using flip chip mounting. To support a common assembly for gate driver and GaN device the existing high temperature SOI CMOS technology will be extended for flip chip mounting. Therefore a base contact to the handle wafer and a modified plug metallization will be developed and implemented in the fabrication flow.

CIRTEM: Design and implementation of isolated GaN drivers with discrete and integrated components for automotive demonstrator and half bridge test vehicle with IZM flip chip.

Task 4.4 System integration (Semikron, CIRTEM)

Intelligent Power Module

Semikron: Complete integration of power devices, SMD components, driver and sensor

functions in an Intelligent Power Modules (IPM) and power systems.

Dual substrate assembly and driver for automotive demonstrator

CIRTEM: Integration of dual substrate sandwich assembly for automotive demonstrator (battery charger). The assembly will include GaN transistors and diodes as well as passive components for EMC and driver purpose. According to the battery charger topology and technological feasibility, there will be one or more assemblies to perform the rectifier and inverter functions of the automotive demonstrator.

Risks and Mitigation of WP4

WP4 provides system integration designs, technologies, characterisation of these and samples for further investigation. Therefore the following risks and mitigations exist.

In case that one project partner is not capable to provide a specified concept, design or characterisation task, there is always a second source available in the consortium as a range of partners is basically capable to provide the whole value chain for WP4 if needed (Semikron, FhG-IMS/IZM, CIRTEM …).

In case that one of the new technologies turns out not to lead to functional samples, there is a fall back solution to provide packages/modules based on standard integration technology. Additionally a detailed cause analysis will give scientific background on the reasons, which will still have a value for further investigations.

#	Deliverable	Owner	Due
D4.1.1	Packaging concepts for the demonstrators Verification: Report on concepts developed from WP 1 specifications and WP 4 objectives	**FhG-IZM,** all WP 4 partners	T0+6M
D4.1.2	GaN modules based on standard technologies Verification: Assembled modules ready for test	**Semikron,** FhG-IZM, CIRTEM, Bosch	T0+15M
D4.1.3	Advanced GaN modules (advanced die bond & flip chip) Verification: Assembled GaN Modules (Test Samples)	**Semikron,** FhG-IZM, CIRTEM, BOSCH	T0+30
D4.2.1	Simulation models of GaN packages/modules Verification: Report on modeling results	**FhG-IZM**, SNPS, UNIVBRIS, BOSCH	T0+18
D4.2.2	First characterization report for different devices, designs and technologies depending from available devices from WP2 Verification: Report on test results regarding thermal and electrical characteristics	**Semikron,** FhG-IZM, EADS, NXP-NL, NXP-UK, SNPS, UNIVBRIS, BOSCH, NANO, CIRTEM	T0+18
D4.2.3	Electrical, thermal and reliability test and simulation report of Packages/Modules Verification: Report on test results	**Bosch,** Semikron, FhG-IZM, EADS, NXP-NL, NXP-UK, SNPS, UNIVBRIS, NANO, CIRTEM	T0 + 36

D4.3.1	First version of integrated gate driver for GaN-devices Verification: Availability of functional Gate driver devices	**FhG-IMS,** Semikron, ST-I	T0 + 17
D4.3.2	Final version of integrated gate driver Verification: Availability of functional Gate driver devices	**FhG-IMS,** Semikron, ST-I	T0+27
D4.4.1	Intelligent power module prototypes for different demonstrators available Verification: Assembled modules ready for demonstrator	**CIRTEM,** Semikron	T0 + 33

#	Milestone	Owner	Due
M4.1.	Preselection of concepts for assembly and drivers Verification: Report available based on prestudies	**FhG-IZM**	T0+6
M4.2	Modules / gate drivers for 1st demonstrator implementation: Verification: Module and gate drivers available for WP5	**Semikron**	T0+18
M4.3	Modules / gate drivers for final demonstrator implementations: Verification: Module and gate drivers available for WP5 (final demonstrators)	**FhG-IZM**	T0+30

	M3	M6	M9	M12	M15	M18	M21	M24	M27	M30	M33	M36
Task 4.1: Packaging Technologies		**M4.1**, D4.1.1										
Standard Assembly					D4.1.2	**M4.2**						
Flip Chip										**M4.3**, D4.2.3		
Advanced Die Bonding										**M4.3,** D4.2.3		
Task 4.2: Thermal Simulation, Characterization and Reliability												
Thermal Simulation & Characterization						D4.2.1						D4.2.3
Thermo-mechanical simulations & characterization						D4.2.1						D4.2.3
Device characterisation and reliability assessment						D4.2.2						D4.2.3
Task 4.3: Electrical and gate driver implementation												
1st version of gate driver development					D4.3.1	**M4.2**						
2nd version of gate driver development									D4.3.2	**M4.3**		
Task 4.4: System integration												
Intelligent Power Module											D4.4.1	
Dual substrate assembly fo automotive demonstrator											D4.4.1	

Work package number	**5**
Work package title	**Application Demonstrators**
Work package leader	**KDEE**

Partner	**ON-semi**	**NXP-NL**	**NXP-UK**	**NXP-B**	**ST-I**	**Semi-kron**	**CIRTEM**	**EPIGAN**	**CISC**
Nat.	BE	NL	UK	BE	IT	DE	FR	BE	AT
PM		**2**	**4**		**36**		**36.3**		**16**

Partner	**NANO**	**EADS**	**MC2**	**IUNET**	**KDEE**	**CEA-LETI**	**FHG**			**STUBA**
							IMS	**IZM**	**IISB**	
Nat.	SK	FR	FR	IT	DE	FR	DE			SK
PM		**8**			**48**			**2**		

Partner	**UNIVBRIS**	**SNPS**	**BIT**	**SE**	**Azzurro**	**BOSCH**	**TU/e**	**AUDI**	**TOTAL**
Nat.	UK	CH	IT	FR	DE	DE	NL	DE	
PM			**36**	**7.5**		**4**	**27**	**7**	**233.8**

Objectives of WP5

This work package is dedicated to demonstrate the potential of GaN-based devices on system level, more precisely via the application demonstrators of GaN-based micro- and string inverters for photovoltaic and electric vehicle battery charger and DC/DC converter for automotive. Additional studies will focus on other potential applications like industrial inverters and innovative designs like switched capacitor converters. Within such context, one of the GaN-based demonstrators will be evaluated for Aeronautic applications concerning EMC requirements.

This work package will include some activities focusing on the most application-specific parameters of the devices like switching performances and losses and will thus be complementary to the characterization effort of WP2 to WP4. The device control strategy will be examined considering constraints at application level like oscillations and over-voltages. A databank with the relevant device performance parameters will be set up for later use in the design and assembly stage. Such information will also be used to benchmark these devices against state-of-the-art Si and also SiC-based devices, with main focus on application relevant properties (to be done in part with activities from WP4), along with the assessment of related gains at system level against the referred devices.

Activities at application level will start with a detailed study of suitable topologies. Aspects to be considered here are the performance assets and constraints of the GaN power devices and how to make best use of it in the target-application. In order to fully demonstrate the potential of GaN devices on application level, further investigations are required:

- The choice and the design of passive filter elements for operation at high switching frequencies (up to several hundred kHz)
- The cooling strategy
- The design of a power/signal board enabling operation at high switching speeds with low levels of electro-magnetic interference

Precise design targets are in the end strongly influenced by the final application. A general list of objectives is nevertheless given as follows:

- Increase in efficiency of the conversion stage (at least by 1%)
- reduction of passive filter elements by means of operation at higher switching frequency (by a factor of at least 2 in size)
- operation at higher junction temperature (in order to reduce costs and dimensions of cooling hardware)
- system cost reduction (due to lower cost of passive filter elements and cooling).

The final experimental validation of the GaN power electronics will be performed via the consideration of experimentally derived overall efficiency, footprint, weight and reliability of the assembled application demonstrator. Such factors will be employed in the end to perform an analysis based on the TCO (total cost of ownership) for selected demonstrators. With such methodology it is possible to benchmark the possible reduction on the hardware investment costs in conjunction with enhanced performance regarding energy consumption (charger / DCDC converter) or generation (PV-inverters).

Description of WP5

The activities in WP5 will be divided in three main tasks, the first two dealing with the application of GaN technology in photovoltaic and automotive conversion systems. The third task group will include more generic investigations about possible future applications.

Task 5.1: Demonstrators for photovoltaic systems [KDEE, ST-I**].**

Task 5.1.1: Photovoltaic-Inverter Demonstrator – design and construction [KDEE].

In a preliminary stage of this task, application-specific properties of the packaged GaN devices will be investigated. Main point of interest is to determine the best trade-off between higher switching speed (in order to reduce switching losses) and possible negative side effects on the application. A databank of the conduction and switching losses of GaN power switches under different conditions will be set up for future use in the design stage. All these activities will take place in close cooperation with WP4. Key-device properties will also be used in a brief comparison of performance features against stage-of-the-art Si and SiC-based devices.

The core objective of the present task is focused on the design of a single-phase photovoltaic inverter having the following specifications. These targets represent a 50% reduction in weight, and improvement of 2% in efficiency compared to current products with silicon devices. An assessment of attainable gains with other new devices based on Si and SiC will also be performed, in order to benchmark the attractiveness of the GaN technology to the application.

- Grid Voltage: 230 Vrms
- Grid Frequency: 50 Hz
- Output Current: 22 Arms
- Input voltage range: 175 – 500 Vdc
- Maximum Output Power: 4500W
- Efficiency: > 98.5%
- Cooling: natural convection
- Weight: <13 kG
- Volume: <15 lt

In a first step of the development, the most suitable topologies of converters for string-inverters rated up to 4.5kW will be chosen and investigated into a preliminary design aiming to identify the application benefits through the use of GaN power devices.

Simulation of the power circuit and detailed design will be performed for the selected converter. Special attention will be given to determine the optimal switching frequency defining the best

trade-off between efficiency and the final cost/size. Due to the multi-dimensional nature of such an investigation, approaches like the pareto-optimization algorithm will be employed.

The design of the power board, control and sensors will need to be carefully considered in order to deal with increased levels of switching speed required for operation at higher switching frequency. Expected here are transients up to 5A/ns and 100V/ns.

Three generations of demonstrator prototypes will be constructed and assessed in terms of efficiency (as a function of voltage and temperature), but also EMC behavior. The first prototype will make use of commercially available devices in order to have one early prototype for learning purposes, serving as benchmarking against the GaN-based demonstrators developed during the project. With the availability of project devices, two generations of GaN-based demonstrators will be built – the first one with discrete power devices and driving circuitry and the second one with integrated intelligent power module (with driving and sensors).

Task 5.1.2: Photovoltaic Micro-inverter Demonstrator – design and construction [ST-I]

An investigation on circuit topologies for micro-inverters will be carried out with the aim to define the best solution for GaN technology exploitation. The rated power is around 300W, which is typical for PV panel nominal power. Further specifications are given below. These targets represent a 33% reduction in weight, and improvement of 1% in efficiency compared to current products with silicon devices.

- Grid Voltage: 230 Vrms
- Grid Frequency: 50 Hz
- Output Current: 1.1 Arms
- Input voltage range: 20 – 50 Vdc
- Maximum Output Power: 250W
- Efficiency: > 95%
- Cooling: natural convection
- Weight: <1kg

In particular, the optimal switching frequency (higher than 100kHz) will be selected taking into account the efficiency as well as size/volume and cost. The optimal driver circuit for GaN power devices (MOSFET) will be designed and implemented within WP4 for both low and high voltage devices.

After detailed simulation, a prototype will be designed and realized. The prototype will be fully debugged and characterized under the whole operating range.

This micro-inverter may possibly be further assessed by EADS to evaluate its compatibility with EMC Aeronautic requirements.

Task 5.2: Demonstrators and studies for automotive systems [CIRTEM, AUDI, BIT, CISC, EADS**].**

Task 5.2.1: Automotive-Converter Demonstrator [CIRTEM, AUDI].

The aim is to build an on-board 3.5KW battery charger for Hybrid/Electrical Vehicles. This isolated AC/DC converter is supplied by the domestic power network and provides the energy to the power battery of an electric vehicle. This demonstrator will integrate the technologies developed in WP2 and WP4 (Power modules with GaN dies, driver…). Two development cycles are planned to reach the final prototype that will be tested according to the specifications below. These targets represent a 60% gain in weight, 45% in volume and 3% in efficiency compared to current products with silicon devices. Thanks to natural convection cooling, moving parts or leaking coolant cannot affect the reliability.

- Input Voltage: 100 - 240 Vrms
- Input Frequency: 47 – 63 Hz

- Maximum Input Current: 16 Arms
- Input Power Factor: > 0.98
- Output Voltage: 225 – 450 Vdc
- Maximum Output Power: 3500W
- Efficiency: > 97%
- Cooling: natural convection
- Weight: <3 kG
- Volume: <3 lt

To use the maximum power available on a domestic electrical outlet without disturbing the mains, the converter should absorb a sinusoidal current (Power Factor correction function) and maximize its efficiency. For safety reasons, the output of the converter (i.e. battery) must be isolated from the mains.

As the converter is on board, its volume and weight should be as low as possible. These characteristics can only be obtained with switching converters. Such converters are composed of active (diode, transistor) and passive (capacitor, inductor, and transformer) components. Adjusting the power transfer is achieved by pulse width modulation at the switching frequency. The volume and the weight of the passive components are roughly inversely proportional to the switching frequency while losses in active components are proportional to this frequency.

Because of thermal limits, the reduced volume and weight is only possible with increased efficiency. This implies a reduction of losses in active and passive components while increasing the switching frequency. Thanks to its low specific on-state resistance and extremely low switching times, the 600V GaN High electron mobility transistor (HEMT) is particularly well suited to achieve these goals unfeasible with silicon components.

In the second design cycle, CIRTEM will work together with AUDI. In the development phase, AUDI will provide hardware reviews to incorporate automotive lessons learned, i.e via schematic, layout, thermal performance and subcomponent qualification reviews. Furthermore, an automotive short product validation & short design validation of demonstrator will be performed including vibration & shock testing, temperature shock testing, temperature cycle testing (test planning, building of test & monitoring equipment, setting up tests, performing tests, evaluation of collected data, test report). Finally, performance bench testing will be performed in an electric vehicle.

Task 5.2.2 DC/DC converter for automotive [BIT,CISC]

The goal will be to test the GaN devices by adapting the design of a DC/DC converter for automotive, to fit the technologies being developed in WP2 and WP4 with the aim to reduce the dimensions and increase the efficiency of the present Si-based technology.

The preliminary specifications of the target application are summarized here

- DC-link voltage 200-400V (high voltage side)
- DC nominal output voltage: 14V (low voltage side)
- Power rating 1.4kW
- Switching frequency: ≥200kHz
- Losses reduction of around 30%
- 30% reduction in size

This in turn is defining some preliminary requirements for the GaN power devices under development which can be summarized as follows and will be detailed inside the WP1:

- Ratings: 600V, 20A
- Package: better if D2PAK or similar
- Interface to the Gate driver board, protection strategies, to be defined jointly

CISC will in parallel perform modeling and simulation work for the design of the power converter system. System level requirements will be verified by advanced simulation

capabilities and models within a simulation framework to evaluate the advantages of GaN technology on system level. Inputs for modeling will be taken from WP2 and WP3. Inputs for the simulation targets will come from the application partners. The approach will be done in 4 steps:

- Develop the component models for system level simulation
- Develop an converter model showing the technology effects on “system” (=converter Level)
- Include the converter model in an application simulation
- integrate within existing simulation framework
-

Task 5.2.3: Evaluation of existing converter for Aeronautic applications concerning EMC requirements [EADS]

This task consists in performing EMC studies at the EADS facilities to check the suitability of these GaN-based demonstrators with EMC Aeronautic requirements.

By default, the DC/DC converter of task 5.2.2 as provided by BIT will be used for this study. Alternatively, the photovoltaic micro-inverter of task 5.1.2 could be used.

Task 5.3 Preliminary studies on industrial converters and other applications [SE, TU/e**].**

Task 5.3.1: Power inverter demonstrator [SE]

The objective is to build a 1KW power inverter for testing GaN devices performances and investigate the optimum between efficiency, maximal switching frequency and reduction of passive filtering devices. Preliminary specifications and targets are given below.

- Input Voltage: 400 DC
- Switching frequency: from 20kHz to 500KHz
- Rated power: 1kW
- Output voltage range: 120V AC
- Efficiency: > 98.5% compared to equivalent demonstrator with Silicon devices
- Volume: 70% reduction of passive devices size at 500kHz operating frequency compared to demonstrator operating at 20KHz switching frequency

The demonstrator will integrate technologies developed in WP2 and WP4 (Power modules with GaN dies, driver…). Moreover, investigation will be carried out on paralleling of GaN devices in order to increase the power rating of the converter.

Task 5.3.2: Switched Capacitor Converter (inductor-free based converter) [TU/e]

At the initial step of the concept development, the most suitable topologies of switched capacitor converters (SCC) with an inductor-free based design with high efficiency operation for rated up to 1kW will be researched. Different topologies with low voltage loads that need to be powered from a low voltage source in the range of 40-50 V (including possible bi-directional power controlling feature e.g. for automotive applications) will be chosen and investigated into a preliminary design aiming to identify the application benefits through the use of GaN power devices. Current spikes, as encountered in the first generations of SCC, are not causing a real problem when it is feasible to switch really fast (very low ripple voltage on the capacitors). This brings to a potential opportunity to use GaN devices.

A new analysis method will be proposed and developed with the aim to reduce the order of complicated network-based formulations and decrease a computational time. Extended simulation of the power circuits and detailed design will be performed for the selected converter topology aiming at prediction and minimization of power required to drive the switches (the gating loss) and the losses due to the presence of the parasitic elements like stray capacitances to ground or resistances in the conduction path and etc.). Special attention

will be given to determine the optimal switching frequency defining the best trade-off concerning efficiency and the final cost/size.

Because for a given ON-resistance, the GaN die size becomes very small, it is expected that, certainly for economic semiconductor manufacturing reasons, multi-switch packages will become available. Combined with the fact that because of mechanical stress reasons piezo-electric transformers are limited to about 15 Watts maximum, this means that for higher power output distributed multi-switch, multi-transformer topologies are needed. Currently, these challenging topologies are not subject to research.

Risks and Mitigation of WP5

- Devices do not meet specifications (regarding threshold levels, driving levels limitations, high leakage) → mitigation with new driver designs and techniques
- High temperature device instability → mitigation by means of discussion of possible enhancements on packaging and coupling with cooling system
- High level of EMI due to high switching speed → mitigation with new board designs, EM-Filtering alternatives, reduction of switching speed
- Devices not available : use alternative GaN components to continue investigations at system level

#	Deliverable	Owner	Due
D5.1.1	Intermediary design of demonstrators for photovoltaic (inverter and microinverter) Verification: hardware, final report with performance data (efficiency and other measurements) and design issues	**ST-I,** KDEE	T0+24
D5.1.2	Final design of demonstrators for photovoltaic (inverter and microinverter) Verification: hardware, final report with performance data (efficiency and other measurements) and critical discussion	**KDEE,** ST-I, EADS	T0+36
D5.2.1	Intermediary design of automotive-converters (battery charger and DC-DC converter) Verification: hardware, final report with performance data (efficiency and other measurements) and design issues	**CIRTEM,** BIT	T0+24
D5.2.2	Final design of automotive-converters (battery charger and DC-DC converter) Verification: hardware, final report with performance data (efficiency and other measurements) and critical discussion	**CIRTEM,** AUDI, BIT, EADS	T0+36
D5.2.3	Results of the modeling and simulation work for design of power converter for automotive Verification: report with discussion of results	**CISC**	T0+36
D5.3.1	Results of the investigations with switched Capacitor Converter and related topics Verification: report with discussion of results	**TU/e**	T0+30
D5.3.2	Power Inverter design with 2nd Generation of project devices Verification: hardware, performance data (efficiency and	**SE**	T0+36

	other measurements), final report with discussion of results		

#	Milestone	Owner	Due
M5.1	Preliminary results of 1st demonstrators based on Gen 1 devices: Verification: 1st full learning cycle completed: feedback to WP2-4	**ST-I**	T0+22
M5.3	Final evaluation of photovoltaic inverters (string and micro): Verification: Hardware + test report (efficiency,..) available	**KDEE**	T0+36
M5.2	Final evaluation of Automotive Demonstrator (battery charger / DC/DC converter) Verification: Hardware + test report (efficiency,..) available	**CIRTEM**	T0+36

Demonstrator collaboration matrix

In the table below are presented the individual demonstrators, assigning the related tasks and components to the project partners

	Components / Design				
Owner	**Power devices (discrete)**	**Power devices (module)**	**Driving**	**Power converter design**	**Power converter testing**
KDEE	NXP	NXP+ Semikron	KDEE+ Semikron	KDEE	KDEE
CIRTEM	ONsemi/ backup NXP	CIRTEM	CIRTEM	CIRTEM / AUDI	CIRTEM / AUDI
ST-I	ST-I	-	ST-I	ST-I	ST-I
SE	CEA (and other?)	CEA (and other?)TBD	TBD	SE	SE
BIT	NXP ST-I	NXP ST-I	BIT -ST-I	BIT	BIT

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WP5 - Application demonstrators

Task 5.1: Demonstrators for photovoltaic systems	**M3**	**M6**	**M9**	**M12**	**M15**	**M18**	**M21**	**M24**	**M27**	**M30**	**M33**	**M36**
Photovoltaic-Inverter Demonstrator – design and construction							**M5.1**	D5.1.1				**M5.3**, D5.1.2
Photovoltaic Micro-inverter Demonstrator – design and construction												

Task 5.2: Demonstrators and studies for automotive systems	**M3**	**M6**	**M9**	**M12**	**M15**	**M18**	**M21**	**M24**	**M27**	**M30**	**M33**	**M36**
Automotive-Converter Demonstrator							**M5.1**	D5.2.1				**M5.2,** D5.2.2
DC/DC converter for automotive												**M5.2**, D5.2.2,D5.2.3

Task 5.3 Preliminary studies on industrial converters & other	**M3**	**M6**	**M9**	**M12**	**M15**	**M18**	**M21**	**M24**	**M27**	**M30**	**M33**	**M36**
Pow er inverter demonstrator												D.5.3.1
Sw itched Capacitor Converter (inductor-free based converter)										D.5.3.2		
Evaluation for Aeronautic applications concerning EMC requirements												

Work package number	**6**
Work package title	**DISSEMINATION AND EXPLOITATION**
Work package leader	**UNIVBRIS**

Partner	**ON-semi**	**NXP-NL**	**NXP-UK**	**NXP-B**	**ST-I**	**Semi-kron**	**CIRTEM**	**EPIGAN**	**CISC**
Nat.	BE	NL	UK	BE	IT	DE	FR	BE	AT
PM	**1**	**2**		**2**			**1**	**2**	**2**

Partner	**NANO**	**EADS**	**MC2**	**IUNET**	**KDEE**	**CEA-LETI**	**FHG**			**STUBA**
							IMS	**IZM**	**IISB**	
Nat.	SK	FR	FR	IT	DE	FR	DE			SK
PM	**1**	**2**	**1**	**2**	**2.5**	**1.5**	**2**	**2**	**2**	**3**

Partner	**UNIVBRIS**	**SNPS**	**BIT**	**SE**	**Azzurro**	**BOSCH**	**TU/e**	**AUDI**	**TOTAL**
Nat.	UK	CH	IT	FR	DE	DE	NL	**DE**	
PM	**2.5**	**1**		**0.5**			**1**		**34**

Objectives of WP6

The main objectives of this work package deal with all activities related to the dissemination and exploitation of the project results. The first part of this work package deals with all the issues related to the dissemination of the project progress and the achieved results to a broad audience, including engineers and scientists from industry and SME's, as well as researchers, instructors and students from educational institutions and research centres. Various parallel dissemination routes will be taken such as publications in key international scientific journals, and presentations at major national and international conferences and meetings, and the set-up and maintenance of a project web-site to enable wide impact and visibility of the project. The dissemination will also include key high-profile workshop organized by the consortium with external contributor attendance. We also envision an interactive e-learning lecture module on "Advanced Power Devices" to be prepared as a complementary part of a regular education process and/or study material for Life Long Learning and/or retraining of experts from industry. The second part of this work package is related to the exploitation of the project results. The exploitation activities include advertisement and promotional activities for awareness creation about the outcomes of the project, as well as the preparation of the exploitation plans by the individual partners and by the Consortium as a whole. Besides these activities, market analysis and roadmapping will be part of the exploitation tasks.

Description of WP6

Task 6.1: Set-up and maintenance of the project web-site (TL: NXP-B)

The objective of this task is the set-up and maintenance of a public web-site. The web-site will be the main point of collection of the project information, including public deliverables, summary of major scientific achievements, advertisement, and dissemination activities. Maintenance and updates will take place on a regular basis (monthly), while major revisions and restructuring will occur on a six-monthly basis. The web-site will contain a private

password-protected section which will be reserved for communication and data sharing within the consortium. The web-site will be managed by the project coordinator.

Task 6.2: Dissemination (TL: UNIVBRIS)

The partners of the E²COGaN consortium will disseminate the project results through various means, including scientific presentations at international conferences, meetings and workshops, publication of papers in international journals, magazines and conferences, participation to activities such as tutorials, panels, round tables and seminars in international events, as well as to summer courses and targeted dissemination actions regularly organized by the scientific community. It is expected that the project will generate a large amount of innovative, scientifically sound research results, which could lead to many high impact internationally leading journal publications and conference presentations. A measure of success of the scientific impact of the project will be the number and quality of the papers published jointly by the partners, contributions to leading international conferences and invites presentations by the partners. A dissemination plan will be prepared and issued at the beginning of the project, and updated at month M18 to maximize impact of the project at a time when the maximum scientific and technical output can be taken advantage of. It will serve as reference for the execution of the dissemination activities.

Relevant conferences and workshops we target for are specialized compound semiconductor conferences in particular IEEE IEDM, IEEE IRPS, IWN, ICNS, ICSCRM, ECSCRM, ESREF, ESSDERC, HETECH, WOCSDICE, SOTAPOCS, MANTECH, ESA Round Table, and ROCS, also more diverse meetings and symposia like the ECS, MRS, E-MRS, with priority of "top-notched" electronic conferences, in particular IEEE IEDM and IEEE IRPS. Results of will also be presented at conferences such as IEEE ECTC, IMAPS (packaging), HITEC, HiTEN (high temperature electronics) or CIPS, PCIM, EPE/ECCE (power electronics). A special session devoted to presentations of the results obtained in E²COGaN is anticipated within the ASDAM (Advanced Semiconductor Devices and Microsystems) conference in 2014, with this activity coordinated by STUBA. Two other special sections with special focus on the results obtained at application level (with the demonstrators) are aimed to be organized in the 16th European Conference on Power Electronics and Applications (EPE/ECCE, with a more academic audience) in 2015 and in the PCIM 2015 (industrial audience), with this activity coordinated by KDEE. Another possibility being targeted is organizing a Workshop together with the ECPE (European Center for Power Electronics) focusing on GaN-Technology application in power electronics systems. For such purpose, participants of the project that are "Competence Centers" of the ECPE will take a leading role in the organization and topics.

Relevant magazines and scientific journals we target for:

- IEEE Transactions on Reliability
- IEEE Transactions on Electron Devices
- IEEE Electron Device Letters
- IEEE CPMT Transactions
- IEEE Transactions on Power Electronics
- IEEE Transactions on Industrial Electronics
- IEE Electronics Letters
- Microelectronics Reliability
- Applied Physics Letters,
- Journal of Applied Physics
- J. Vac. Sci. Technology
- EETIMES (EETIMES Europe)
- Compound Semiconductors
- Semiconductor Today
- Solid State Electronics
- APEX

The dissemination plan will also include a targeted workshop at the site of the project coordinator of all the partners of the project, open to external interested parties, for high public relation impact of the project, and as milestone for external project input to benchmark the project progression and success.
Implementation of obtained results in the field of advance power devices using new materials and disruptive technologies into educational process will have a wide impact on the preparation of new generation of highly educated experts which are needed for further development of innovative technologies in the future. STUBA will prepare an interactive e-learning lecture module on "Advanced Power Devices" as a complementary part of a regular education process and/or study material for Life Long Learning and/or retraining of experts from industry.

Task 6.3: Exploitation (TL: NXP- B)

In order to implement a successful exploitation strategy, the partners of the E^{2}COGaN project, as well as the Consortium as a whole, will take the appropriate actions and measures already during the project lifetime to prepare for the successful exploitation of the project results. All the industrial partners in the project will prepare result exploitation plans, indicating in detail what market and business opportunities will be favoured by the development of the new technologies made in the E^{2}COGaN project. A preliminary plan, jointly compiled by the Consortium as a whole and by each individual partner will be delivered at M18. The exploitation plan will then be finalized at the end of the project.

Risks and Mitigation of WP6

Risk of no publications or no new results emerging from this project, risk of international competitor new IP emerging. This is an extremely unlikely scenario considering the strength of all the partners of this project. Lack of publications and new results will be addressed, in the unlikely case, via the management committee of this project. The internationally IP situation will be continuously be assessed as part of the exploitation plan developments of this project, and strategic decisions will be taken by the management committee of this project, if necessary.

#	Deliverable	Owner	Due
D6.2.1	Activity report on publications and presentations. Verification: Delivery of report	**UNIVBRIS,** All Partners	T0+12
D6.2.2	Activity report on publications and presentations. Verification: Delivery of report	**UNIVBRIS,** All Partners	T0+24
D6.2.3	Activity report on publications and presentations including initial exploitation successes Verification: Delivery of report	**UNIVBRIS,** All Partners	T0+36

#	Milestone	Owner	Due
M6.1.	Set-up of public/internal E^{2}COGaN website: Verification: Web-site operational	**NXP-B**	T0+3

M6.2	Updated exploitation plan: Verification: Updated Report available	**NXP-B**	T0+18
M6.3	E²COGaN Workshop: Verification: 1-day workshop organized	**UNIVBRIS**	T0+27

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	M3	M6	M9	M12	M15	M18	M24	M27	M30	M33	M36
Task 6.1: Set-up and maintenance of the project web-site	**M6.1**										
Task 6.2: Dissemination				**D6.2.1**			**D6.22**	**M6.3**			**D6.2.3**
Task 6.3: Exploitation						**M6.2**					**D6.2.3**

All partners contribute to this work package and the tasks 6.2 and 6.3, and provide critical input to task 6.1.

Work package number	**7**
Work package title	**Project Management**
Work package leader	**NXP-B**

Partner	**ON-semi**	**NXP-NL**	**NXP-UK**	**NXP-B**	**ST-I**	**Semi-kron**	**CIRTEM**	**EPIGAN**	**CISC**
Nat.	BE	NL	UK	BE	IT	DE	FR	BE	AT
PM	**12**	**1**	**1**	**1**		**1**		**1**	

Partner	**NANO**	**EADS**	**MC2**	**IUNET**	**KDEE**	**CEA-LETI**	**FHG**			**STUBA**
							IMS	**IZM**	**IISB**	
Nat.	SK	FR	FR	IT	DE	FR	DE			SK
PM	**1**			**1**				**1**		**1**

Partner	**UNIVBRIS**	**SNPS**	**BIT**	**SE**	**Azzurro**	**BOSCH**	**TU/e**	**AUDI**	**TOTAL**
Nat.	UK	CH	IT	FR	DE	DE	NL	**DE**	
PM	**1.3**	**0.5**		**0.5**		**1.5**	**1**		**25.8**

Objectives of WP7:

The major objective of this work package is to guarantee that the goals of the E^{2}COGaN project, as described in the project proposal, are achieved within the planned time and budget. The work to be performed in this WP includes: Set-up and implementation of all the project management structures, as described in Section 7.1; organization of the project kick-off meeting and of the periodic management and technical meetings; execution of day-by-day project administration and monitoring of work progress; technical steering of the project; identification of potential risks and definition of appropriate recovery plans; monitoring of the performance of the consortium partners; implementation of corrective actions to cope with possible misbehaviour of partners; definition of standards, procedures and conventions regarding matters such as documentation and review procedures; preparation and delivery to the ENIAC JU of the required documents and reports; organization and preparation of the project review meetings; preparation of the consortium Agreement document which, among other matters, will set-up proper policies and guidelines for intellectual property protection, internally and externally to the consortium.

Description of WP7:

Task 7.1: Implementation of project management structures

(Participants: NXP-B, Start: M1 – End: M36)
The main objectives of this task is for the project coordinator to set-up and implement the necessary project management structures in accordance with the scheme described in section 7.1. In addition, the project coordinator will organize the project kick-off meeting no later than one month after the start of the project.

Task 7.2: Project management

(Participants: NXP-B, All, Start: M1 – End: M36)
In this task, the project coordinator and all the partners will perform the due project management activities, as described in Section 7.1 of this proposal. Such activities include

technical, strategic, administrative and financial actions, all devoted to an efficient, on-time execution of the project work and the delivery of the corresponding results. Key tool for project management will be the Internal Project Web Site. It will be used to manage the contact and distribution lists, as well as a repository for communication and documentation exchange among the partners. Part of the project management is the duty of the project coordinator to be the primary contact point to the ENIAC JU and the reviewers for all the matters, technical and administrative, concerning the execution, progress and management of all project activities. Any action concerning communication to the ENIAC JU and the reviewers, as well as the exchange of material, technical, administrative and legal documents occurs in the context of this task.

Task 7.3: IPR Management

(Participants: NXP-B, All, Start: M1 – End: M36)

This task concerns the establishment of appropriate policies and rules for the management of background and foreground IP for the technologies developed within the E^{2}COGaN project. As common practice in the recent past government funded projects the activity will converge in the Consortium Agreement in which the partners shall define the guidelines for information exchange of pre-existing know-how. IPR management will be a continuous activity covering the entire project lifetime, collecting a list of reusable and non-reusable pre-existing know-how available at the start of the project, and new know-how generated by the R&D activities during the project.

#	Deliverable	Owner	Due
D7.2.1	1st half year report Verification: Delivery of report	**NXP-B,** all	T0+6
D7.2.2	2nd half year report Verification: Delivery of report	**NXP-B,** all	T0+12
D7.2.3	3rd half year report Verification: Delivery of report	**NXP-B,** all	T0+18
D7.2.4	4th half year report Verification: Delivery of report	**NXP-B,** all	T0+24
D7.2.5	5th half year report Verification: Delivery of report	**NXP-B,** all	T0+30
D7.2.6	6th half year report Verification: Delivery of report	**NXP-B,** all	T0+36

#	Milestone	Owner	Due
M7.1.	Project management set-up Verification: Management procedures in place	**NXP-B**	T0+6
M7.2	Project management activities, intermediate review Verification: Mid-time review successful	**NXP-B**	T0+18
M7.3	Management activities, final review Verification: Final review successful	**NXP-B**	T0+36

6.3 Description of milestones and demonstrators

The overall logic behind the set of the E²COGaN milestones is the use of two complete learning cycles or integration waves, that are realistically required to reach the highest project goals at t0+36, which are industrially relevant demonstrators for both solar (M5.2) and automotive applications (M5.3). The explicit ambition at the end of this project is to have demonstrators that are not only fully operational but also capable to validate the promises of GaN power electronics in terms of high efficiency, compactness and competitive cost on system level.

During the 1st learning cycle the most critical milestones are the first set of functional requirement specifications at t0+5 (M1.1), the availability of devices at t0+12 (M2.2), first assembly and gate driver results at t0+18 (M4.2) and first assembly of the application demonstrators at t0+22 (M5.1). The combined learning through all involved WPs will be mandatory input for a refinement of the specifications at t0+18 (M1.2), the availability of 2nd generation devices at t0+24 (M2.4), their use in assembly at t0+30 (M4.3) and the final validation in the end application demonstrators at t0+36 (M5.2/3).

Concerning the two main application demonstrators, the following critical paths have already been defined:

For the photovoltaic inverter demonstrator, 600V capable GaN epitaxy substrates will be made available by EPIGAN and AZZURRO (M2.1). NXP will have the main responsibility (with ONsemi as back-up provider) of the GaN device manufacturing for the 1st (M2.2) and 2nd generation (M2.4) for further use in the power modules, provided together with the default gate drivers by Semikron (M4.2) and - for a later generation - by FHG (M4.3). The final design, assembly, testing and validation of the PV application demonstrators (string and micro-inverter) will be carried out under the lead of KDEE and ST-I (M5.2).

Concerning the automotive application demonstrator, ONsemi will provide the GaN power devices (with NXP as back-up supplier) complying to the specs previously defined (M1.1 / M1.2) for the 1st (M2.2) and 2nd generation (M2.4). Default module and gate driver development will be carried out by CIRTEM (with Semikron as back-up, M4.2 and M4.3) who is also in charge of design, assembly and testing of the final demonstrator, a 3.5kW battery charger for electrical vehicles (M5.3).

Final validation of the demonstrators will be two-fold: by availability of the hardware itself and by a report including efficiency tests and system cost estimation for direct comparison with incumbent Si or SiC solutions.

The table below gives a complete overview of the milestones associated to the major and most critical expected results during the duration of E²COGaN.

TABLE 2: LIST OF MILESTONES

Milestone no.	Milestone name	WPs no's.	Lead beneficiary	Scheduled Delivery Date
M1.1	Application-driven functional requirement specs for epi, device and module	1	ONsemi	T0+5
M1.2	Review of functional requirement specs	1	ST-I	T0+18
M2.1	1st Generation 800V epi-substrates	2	AZZURRO	T0+6

M2.2	1st Generation 600V power devices , D-mode	2	NXP-UK	T0+12
M2.3	Optimised 6" and 8" epi-wafers (R_{SH} <250 Ω/sq)	2	EPIGAN	T0+18
M2.4	Optimized 600V power devices (D-mode):	2	ONsemi	T0+24
M2.5	Final conclusion on advanced GaN devices: e-mode and 1.2kV devices	2	CEA LETI	T0+36
M3.1	Conclusions on screening of failure modes and thermal limitations in GaN Power devices	3	UNIVBRIS	T0+18
M3.2	Simulation approach for reliability investigation and lifetime predictions in GaN power device	3	SNPS	T0+24
M3.3	Most relevant failure modes and device limitations understood and recommendation list for reliability improvement	3	IUNET	T0+24
M4.1.	Preselection of concepts for assembly and drivers	4	FhG-IZM	T0+6
M4.2	Modules / gate drivers for 1st demonstrator implementation	4	Semikron	T0+18
M4.3	Modules / gate drivers for final demonstrator implementations	4	FhG-IZM	T0+30
M5.1	Preliminary results of 1st demonstrators based on Gen 1 devices	5	ST-I	T0+22
M5.2	Final Evaluation of photovoltaic inverters (string and micro)	5	KDEE	T0+36
M5.3	Final evaluation of Automotive Demonstrator (battery charger / DC/DC converter)	5	CIRTEM	T0+36
M6.1	Set-up of public/internal E2COGaN website	6	NXP-B	T0+3
M6.2	Updated exploitation plan	6	NXP-B	T0+18
M6.3	E2COGaN Workshop	6	UNIVBRIS	T0+27
M7.1	Project management set-up	7	NXP-B	T0+6
M7.2	Project management activities, intermediate review	7	NXP-B	T0+18
M7.3	Management activities, final review	7	NXP-B	T0+33

7.1 Impact

7.1.1 Market Relevance and Economic Impact

A. GaN in the Power Electronics Semiconductor Industry

Within the semiconductor industry, the power electronics sector alone accounts for more than 10% of the total sales with an estimated revenue of 33 B$US in 2011. Moreover, iSuppli foresees an annual growth rate of about 7.2% outperforming largely the semiconductor average for the next years. This reflects the increasing societal and economic needs in terms of efficient and intelligent energy generation, transmission, storage and end usage especially in Europe and other highly developed regions of the world.

As emerging and disruptive power semiconductor technology, GaN is likely to change the rules of the power semiconductor market over the next 20 years. Over the last 15 years a great effort has been spent to establish SiC as the next power generation technology in the 600-1800V range. Indeed, SiC has proven to bring a significant advantage in terms of efficiency on device (both diode and transistor) and system level. In parallel, a large R&D effort enabled considerable advances in substrate and device engineering and manufacturing. Nevertheless, until now, the SiC technology has not succeeded in a broad market entry, mainly due to the high and only slowly decreasing cost of the starting substrates making the SiC power devices too expensive with respect to the incumbent silicon technologies.

Company	Origin	2010 revenues	GaN/Si	GaN/SiC	SiC
Infineon Technologies	DE	1356	X		X
Toshiba	JP	1155	?	X (for RF)	X
Mitsubishi	JP	1088	?	X (for RF)	X
STMicroelectronics	CH/FR/IT	1000	X	X	X
Vishay Intertechnology	USA	986			?
Fairchild Semiconductor	USA	953			X
Renesas Electronics Corporation	JP	870	X (CATV)		X
International Rectifier	USA	852	X		
Fuji Electric	JP	724	X	?	X
ON Semiconductor	USA/BE	467	X		
ROHM Semiconductor	JP	372	X		X
NXP	NL/UK/BE/DE	323	X	X (for RF)	
Others					
TOTAL		**14,573**			

Source - Isupply

Table 3: Overview on the top 12 power semiconductor companies and their commitment in the Wide-Band-Gap technologies SiC and GaN.

What makes the GaN power device technology so unique is the fact that it has (up to 1200V) similar or even better performance promises as compared to SiC, but at a by far more promising cost-perspective. Through recent advances in the MOCVD growth of GaN on Si (instead of using SiC or sapphire as starting substrates) and the recent commercialization of large multi-wafer epitaxy tools, high quality and cost-efficient substrates at competitive wafer sizes (6” in production, 8” in R&D) are now in reach. Accordingly, WSTS predicts a

Total Accessible Market (TAM) of 8.4 B$US in 2015 and 11.3 B$US in 2020 for GaN power devices. Not surprisingly, at least 10 of the top 12 semiconductor companies have a significant R&D effort on GaN electronics and at least 7 of them work actively towards power diodes and switches based on GaN-on-Si. Even more interesting, nearly all companies having SiC in their power device portfolio take also a bet on GaN – a clear statement that even the strongest believers in SiC cannot longer ignore the recent developments on GaN and its impact on the power semiconductor market over the next 20 years.

For 2012, StrategicAnalysts indicate the total sales in GaN devices of the order of 70M$US, with more than 90% restricted to RF applications in military, wireless and CATV. They consider sales in GaN power devices as negligible today, but forecast an over-proportional growth in the next coming years. Another analyst, Yole, indicates the revenues of GaN power devices of the order of only 10 M$US in 2012, but foresees a tremendous growth to 400 M$US in 2015 and even 1.9 B$US in 2020, corresponding to a yearly growth rate of 90% !

Today's GaN power devices sales are basically supported by EPC (only <200V), International Rectifier (100V and – more recently – 600V), the start-up companies such as MicroGaN and Transphorm (both targeting 600V diodes and switches) and most likely by a 9few Japanese players, such as Fuji, Sanken and Panasonic.

Company	Origin	Diodes	Switch	Status
EPC	USA		<200V, <30A, normally-off	on sale
Fuji/Furukawa	JP		900-1200V	prototypes?
International Rectifier	USA	SBD, 600V	< 100V w/ driver; -600V, MISHEMT in cascode	LV on sale, sampling for HV
MicroGaN	DE	600V SBD (cascode)	600V (cascode)	on sale
Panasonic	JP	?	?	?
Sanken	JP	600V SBD (cascode)	800V, normally-on and -off	probably on sale
Transphorm	USA	600V/2A	600V, normally-off Rdson=0.31/0.18mΩ	on sale

Table 4: Overview on the GaN power device suppliers as today.

Among the most advanced companies on GaN power devices, we find thus a strong domination of Japanese and American actors. If Europe wants to play an important role in the emerging GaN power device market and grab the above described market opportunities, additional efforts have to be spent in a market-driven, product-oriented technology development. In parallel, the European GaN semiconductor players will need to make use of their assets given by the presence of world-class industrial laboratories and institutes and world-class OEMs and end-customers in the Automotive and Energy industry. This is why we propose as essential key success factor an integrated project through the whole value chain including the most relevant research laboratories and institutes in this field.

More precisely, in order to achieve the highest economic impact possible concerning the GaN power device development, we target within this project:

- Industry-driven and market-relevant definition of device specification and requirements
- Close loop between GaN wafer suppliers and GaN IDMs to ensure cost-effective, high quality and large-size GaN epitaxy layers as starting materials

- Close collaboration between world-class GaN reliability experts and IDMs and wafer supply in order to understand the origin and eliminate device instabilities and other threats to device lifetime
- Interaction between module makers and IDMs to achieve highest performance in terms of switching frequency and device stability aligning efforts in eliminating parasitic inductive or capacitive effects in device, packaging and module design

B. GaN in the Solar Industry

Over the last years, the solar industry has steadily grown to one of the major customers for power semiconductor devices requiring high efficiency at affordable device, system and operation cost. The almost exponential growth rates will offer a market in continuous expansion for power devices enabling further cost savings through an economy of scale.

Within the solar industry, GaN is extremely promising to replace Si or SiC switches and diodes as used in solar inverters, needed in order to connect the solar panel – where the electricity is generated – to the grid – where the electricity is distributed and finally transmitted to the end user. Typically a distinction between string inverters (≤10kW) and micro-inverters (≈0.2kW) is done, the latter being directly connected to only one single panel. In both cases the secondary (AC) side - connected to the grid – requires 600-800V devices while the primary side depends heavily on the system (100V in case of a micro-inverter, 600-800V in case of a string inverter).

According to iSuppli research, the shipments in solar inverters in 2011 were at the level of 23.4 GW worth 6.1 B$USD. Low-power string inverters corresponded to share of 47%, what in turn represents roughly more than 1.500.000 units. High power central inverter took 42%, while micro-inverters had so far reached about 1%.

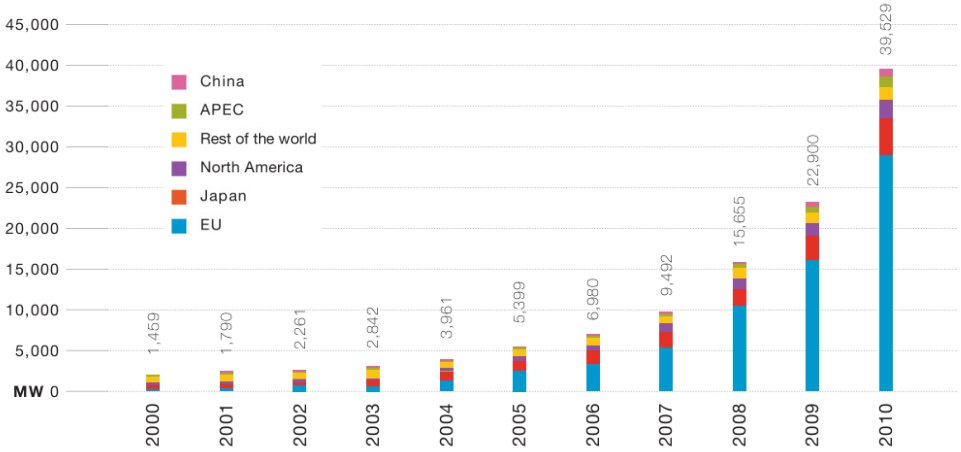

Figure 14: Evolution of global cumulative installed capacity [EPIA].

These values show are slightly in decline with respect to 2010 due to considerable cuts in public subventions especially in Germany and the Czech Republic. While gains are predicted to continue to suffer from decreasing prices, the overall demand is expected to rise again from 2012 reaching sales of 50 GW in 2015. The world-wide supply of solar inverters is dominated by European players with Germany-based SMA alone making up for 30% of the sales.

While low power string inverters still take a significant share of the market, it is possible to observe in the last years a clear trend towards medium and high power-rated inverters, which experienced the highest increase in 2010.

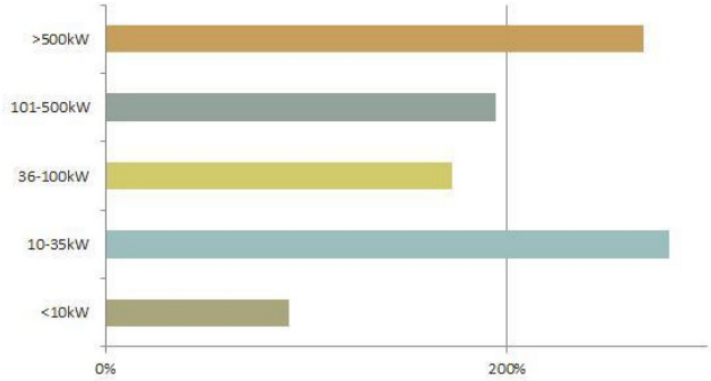

Figure 15: Demand increase in 2010 by inverter power level (IMS Research's Quarterly PV Inverter Report)

Concerning the power level of installed and planned high power systems (above 25MW), it is also possible to observe the trend towards higher power ratings.

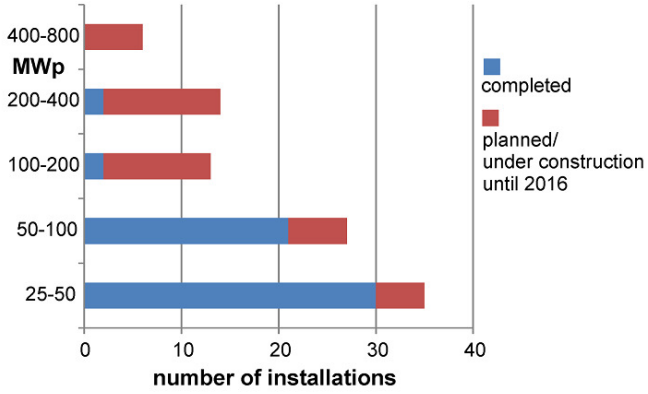

Figure 16: Number of completed and planned photovoltaic power stations [Wikipedia]

In order to maintain Europe's dominant and world-leading position in solar inverters and to ensure that Europe emerges strengthened out of the current solar market crisis, timely investigations to assess the benefit of the emerging and game-changing GaN power technology seem to be appropriate. Prices for inverters based on Si power devices will continue to be under pressure; SiC solutions are capable to bring gains in the overall efficiency but at the price of higher cost of ownership.

The concerted target of the E^{2}COGaN project will therefore be to give proof that GaN can reconcile maximum energy efficiency (which is equivalent to more power fed into the grid) with similar cost of ownership as given by a Si-based inverter system. The high switching frequency capability of GaN - up to 1-5 MHz have been demonstrated in 100V power devices - is one of the key enablers to review the use of passives (and thus reduce cost and footprint) and the overall topology of the inverter. GaN power devices will thus be more than just a silicon replacement: they will enable new concepts and configuration that had not been in reach with incumbent silicon, paving the way to new generations of end products.

For maximum economic impact and highest chance for adoption in a future product, focus will be put on the following items:

- Assessment of alternative, energy efficient topologies enabled by high-frequency switching GaN power devices through simulation and demonstrators

- Review of the whole system (including passives) with a critical view on overall losses, bill-of-materials and footprint
- Collaboration between end-user, system designers and module makers to ensure the best use of the intrinsic GaN device properties
- Early view on lifetime aspects to ensure low cost of ownership in the operation phase
- Relevant final evaluation of the application demonstrator in a field test

C. GaN in Automotive and Transport

The LEV (Light Electric Vehicles) market is expected to evolve step by step, moving to large scale implementation of affordable, safe, ergonomic and clean micro- and mini-cars. The figure below shows how the number of km run in urban mobility, in the first half of the decade, is likely to shift from heavy and polluting vehicles to e-vehicles of much lower weight, including quadri-cycles and other novel forms of mobility. The motivations of that shift are to be searched on a spreading awareness of the finite energy and raw materials resources as well as on the demands for new mobility options. The area below the red curve (electro-mobility) may supplant the area currently covered by conventional vehicles based on internal combustion engines. The economic impact is huge as in Europe by 2020 several millions of new e-vehicle types are expected, with consequent impact on the established supply chains and opportunities for SMEs rapidly pulling through their innovations.

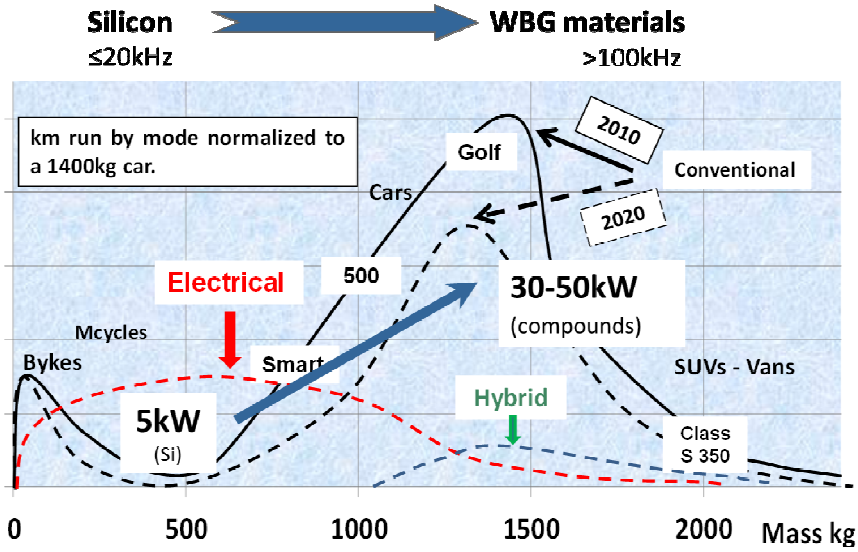

Figure 17: (courtesy of IFEVS Srl, Italy) EU electric mobility towards 2020 50% of bikes, 100% of LEVs (<700kg), 35-40% of vehicles below 1000kg, 8-10% of vehicles around 1400kg are likely to be electric. ICE vehicles are expected to decrease of about 30%. WBG technologies for power conversion (30-50kW, switching frequencies >100kHz) will allow the electrification of larger cars by the end of the decade

A mid-sized EV for urban mobility will be designed such that it can be operated for most of the day by a single charge. On the contrary, on a highway, or more generally at speeds higher than 120km/h, the energy consumption depends mostly on the speed rather than on the distance covered. As a consequence, the association of high speeds and long ranges in a single charge limits the use of hybrid architectures until the next generation when much

more advanced battery technologies and semiconductors becomes available.[1] By 2020, even in the perspective of battery cells with specific energies at 400-450Wh/kg, the cost of the battery pack (~50kWh), needed in heavier than 1400kg cars addressing by a single charge long ranges (~300km) at high speeds (>140kmh), together with the high cost of SiC modules for power conversion, will continue to limit the sales of this category of vehicles to a small percentage of the total. Public institutions, OEMs and suppliers are accelerating their efforts experimenting demonstration car-fleets in many large cities with the purpose to gather data, define best practices and justify the widespread commercialization of electromobility. This will further motivate the adoption of FEVs fleets and spread the awareness of the benefits of electromobility in cities. It is expected that before 2015 most OEMs will be selling electrical vehicles below 1000kg in weight and in the hypothesis that 12-17% of this class of vehicle will be demanded to be electrical, by 2015 the European market will ask for 0,9-1.2 millions of new inverters, battery chargers, DCDC converters[2] (it is here worthwhile noticing that in Europe 17% of the vehicles are sold to public institutions[3]).

GaN devices, expected to enter the mass market at affordable prices by the mid-decade, will allow significant benefits in terms of efficiency for low power on-board conversion devices (solar panel converters, battery charger, DCDC converters), and step-by-step they will be introduced in inverters for the driveline (5 to 10kW) inside LEVs. Once an affordable GaN power semiconductor technologies is available it will be applied and used on a fully electrified passenger car fleet ranging from LEVs for daily usage, to large family cars for long distances.

As today, most of the HV converters contain IGBTs (high power levels) or Super-Junction devices (power levels below 4kW) in combination with Si – or in a more efficient version - SiC diodes for the freewheeling diode. However, further performance increase of IGBTs is increasingly difficult, and switching losses clamp the maximum switching frequency to about 20kHz. Super-Junction devices, especially when targeting above 600V, require complex and cost-intensive epitaxy processes. Here, GaN devices offer less switching losses, higher switching frequencies and up to 10 times smaller device size while having a better cost perspective than competing SiC. Finally, GaN as a wide-band-gap material will enable operation at higher temperatures thus lowering the cooling requirements. All these elements will result in smaller and lighter-weight conversion systems, which is a crucial asset in automotive but also in other sectors (i.e. aeronautics).

For this project, we will focus mainly on the HV battery charger and the internal DC/DC conversion as highly relevant and realistic entry products for GaN power devices in automotive. These applications are key enabling elements for any electric vehicle and contribute thus to pave the road to the cars of the future. Concerning the DC/DC modules a retrofit into conventional cars is thinkable (e.g. using buck / boost converters on a 48V distribution system) giving even a wider economic impact to the proposed solutions.

To increase the economic impact of GaN devices in the selected automotive applications, special focus will be on:

- Identification of the best GaN power device compatible topologies

[1] Most large OEMs seem to be aware of the new demand proposing e-bikes, motorcycles and LEVs of various kind having no rivals amongst ICEVs. See the note on: cars21.com. Urban mobility: small, light and electric, the way to go! 2011-09-28.

[2] Gonzalo Hennequet, Mass Production of EVs: The Technological Challenge of RENAULT, Auto e-motion conference, 27 September 2011, Graz, Austria

[3] Electrification roadmap, Sept 2009. www.greencar.eu

- Robustness in harsh environments (high temperature, etc...) and translation into assembly and cooling requirements
- High efficiency at affordable cost (total bill of materials)
- Compact and light-weight and system solution with respect to incumbent technologies
- Early view on reliability and lifetime aspects
- Extendibility towards aeronautics (250°C, radiation)

The predicted 0,9-1.2 millions e-vehicles with less than 1000kg will represent a significant market. With cost abatement of the battery pack in the coming years the power electronics systems will become very important elements that characterize the value and the technology level of electric vehicles. At a price of 60-70€ per system (battery chargers or DC/DC converters) the direct sales could exceed 100M€. Finally, GaN devices are also likely to enter the traction inverter market, with prices around 250€ per system.

Europe has a leading position in automotive industry and automotive electronics, but facing a very strong competition from the US, Japan and China. This implies the risk that future products will eventually be developed and manufactured in the USA and/or in Far East and subsequently being imported in Europe.

Although Europe has spent a lot of effort in the development of electric vehicles, China is out ahead in the upcoming development. On December 2010 it already had over 160 million electric bikes on its roads and is moving ahead to take the lead as a market for the mobile future. In the next ten years, China's central government will promote electric power trains with massive funding in the order of 1 B€ a year. In turn, the development in China is, therefore, an enormous opportunity for the European automotive industry: it shall join forces and go for becoming a leading supplier in one of the most innovative and value-creative industries on this planet.

The E^2COGaN systems will determine the performance of e-vehicle system-relevant power electronics such as battery chargers and DC/DC converters and their adoption will be a major criterion for a customer to select one EV instead of another. The competitiveness of the overall EU car industry with respect to Asia and the USA will be definitely boosted by the future availability of GaN-based power electronics as explored and assessed in the E^2COGaN project.

7.1.2 Societal Impact

The semiconductor industry generates about 10% of the world-wide and EU-wide GDP and is moreover a key enabler for technological progress in many areas, among them the project-relevant sectors of energy and automotive and other transport, which are also of strategic relevance for wealth and growth in Europe.

In automotive – accounting roughly to 8% of the EU government revenues, electronic components make as today 20% of the car's value which is based on a conventional car with a combustion engine. This percentage is likely to rise with the broad market entry of hybrid or fully electrical vehicles with their higher demands in efficient, cost-effective and light weight motor drives, battery charging and power conversion. The European automotive industry is considered as one of the most competitive in the world thanks to a high innovation rate and advanced manufacturing.

Concerning Energy, Europe is – fuelled by the ambitious EU goals to cut CO_2 emission by 20% until 2020 – leader in many areas of green energy generation, transmission and storage. As an example, Europe is world leader in inverters for solar panels accounting with SMA alone meeting 30% of the world wide demand. Given the need for clean energies, the economic and societal importance of this economic sector will only rise.

The proposed project aiming to demonstrate the disruptive character of GaN power devices in terms of efficiency and cost-perspective through the whole value chain from substrate supplier to end-user will have a two-fold societal impact.

First, it will guarantee and develop Europe's competitiveness and innovation capacity in the areas of semiconductor, automotive and energy industry through an innovative and disruptive power technology. It will contribute to create a European GaN ecosystem securing and providing high quality and sustainable jobs through the whole value chain. Moreover, via the close collaboration between industrial and academic research, a network of excellence on GaN will be one of the outcomes of this project with expected benefits for high level education and development of associated required job skills.

Second, it will contribute to tackle one of the most prominent societal challenges given by the reconciliation of a modern, industrial society and energy efficiency. The targeted application demonstrators in solar and automotive aim at higher power conversion efficiencies than accessible through incumbent silicon at equivalent cost. Their achievement should be thus immediately translated into products that help to maintain the European standard of living while having a positive effect on the overall energy consumption and thus CO_2 emission.

7.2 Dissemination and exploitation

Dissemination and exploitation of the project results are important objectives of the E^2COGaN consortium as a whole, as well as of the individual partners. Over the last 30 years several major breakthroughs have been accomplished in the field of silicon power device architectures such as IGBT and superjunction. However, due to the intrinsic properties of silicon (relatively low bandgap, limited thermal conductivity, etc.) advances in this field have slowed down considerably. It is therefore of the utmost importance that the European industry invests in the research and development of disruptive power device technologies, as based on the Wide-Band-Gap (WBG) materials such as GaN to replace the incumbent Si technologies with the mission to achieve a higher performance at equivalent cost. Consequently, the advances in the GaN-on-Si technology will bring down the cost of high-performance wide-band-gap technology to silicon cost level, and will provide a decisive market advantage for not only the partners in the E^2COGaN project, but this will also translate into a benefit for European companies at large. The E^2COGaN consortium will directly address not only the semiconductor market, but also several end user markets such as automotive, photovoltaic and industrial application markets.

Dissemination plays an important albeit less directly revenue related role for the consortium. First and foremost it generates visibility and underlines the partner's expertise in the area, thus promoting their standing. Furthermore, it also fuels interest in the topic as such, and the partner's technologies and applications. Lastly, dissemination of the project results helps to drive the convergence of the technical state-of-the-art, which in return is a mandatory pre-requisite for a commercially exploitable market. All partners will contribute towards the dissemination of the project results through publications in international, refereed journals and at targeted conferences. Partners will use their contacts to industrial and academic institutions to get an up-to-date picture of the overall market needs and potential of each of the achieved results. Key strategic contributions will be evaluated for patenting.

7.2.1 Dissemination

The E^2COGaN consortium will employ a range of tools to disseminate ideas, concepts and research findings to promote the project and to raise awareness of its progress. Those tools include publications and presentations of papers in journals and at selected conferences, participation to fairs and exhibits as well as the organization of special panel

sessions in distinguished technical conferences. The list of scientific journals and magazines targeted for the publication of some of the E²COGaN technical achievements include: Journal of Applied Physics, Physica Status Solidi, Transactions on Electron Devices, Electron Device Letters, Applied Physics Letters, Microelectronics Reliability, Transactions on Device and Material Reliability. With respect to conferences and symposia, the target list includes: IEDM, IRPS, ISPSD, ESREF, ESSDERC, MRS, APEC, EPE, WOCSDICE, WOCSEMMAD, TWHM, HETECH, CSMANTECH, ROCS, IIRW, HiTEN, HiTEC, CIPS, EUROSIME, ESSCIRC, IWN, ICNS. In addition, the partners will also publish articles in general-purpose and technical news media, both in print and in electronic form on the Internet.

The E²COGaN consortium includes a number of organizations world-wide recognized and their members are represented in most of the key conferences in the nanoelectronics field. This will help in broadening the dissemination of the E²COGaN results in the scientific and industrial communities of IC manufacturers, assembly and users.

E²COGaN will have a strong on-line presence; its own web-site will provide both a public face for the project and private facilities for partners and collaborators. The private site will offer the partners with central repository information and collaborative tools to support distributed problem-solving. The public site will provide contact information, educational material, partners' expertise, activities, and relevant publications, as well as means for engaging the wisdom of experts around the world.

7.2.2 Exploitation

Due to the nature of the project, the exploitation of the project results is not expected to start in the early stages of the project, but rather towards the end of the project. However, the E²COGaN consortium will already take the necessary measures during the lifetime of the project to plan and prepare properly for the exploitation of the project results. From the industrial point of view, innovation expected to come out of the E²COGaN project will result directly in opportunities for each of the participating EU member states.

A summary of the individual industrial partner exploitation activities is presented in the following table, which will be used as a template for a detailed exploitation plan which will be prepared at the early stages of the project.

Beneficiary	Exploitation Plan
NXP-B	NXP will use the outcome and the results of this project to accelerate its market entry concerning GaN HV HEMT and SBDs with first products foreseen during 2014 and to prepare the 2nd generation products for automotive and solar. The GaN production will be carried out in the in-house 6" Si facility in Hazel Grove Manchester where GaN products will gradually replace mature Si MOSFET technologies in the product line, securing and increasing employment in semiconductor manufacturing at this site (currently 400 people, 1100 wafers /day) for the next 20 years. The ramp-up of the GaN production will necessitate broad R&D support to the benefit of the Central R&D organization spread over Eindhoven (NL) and Leuven (BE) and other support functions in the Netherlands (e.g. characterization labs, failure analysis). GaN is regarded as one of the key technologies to position the company in the domains of energy and automotive, but also consumer, RF and telecommunications. In the power electronics domain, NXP forecasts revenues of $20M (2015), $62M (2017, $152M (2020) resulting in a 10% market share of the global GaN power business, driven by Enterprise Systems, Lighting, PFC, Solar and Automotive applications.
NXP-NL	
NXP-UK	

ONSemi	ON Semiconductor intends to use the results of the E^{2}COGaN project to penetrate the market of GaN transistors and rectifiers for high-end applications. Examples of high-end applications are e.g. power switching, power supplies and power conditioning where significant gain in efficiency over conventional silicon devices is possible (e.g., in buck converters) and it is possible to operate at higher frequencies, higher power densities and higher temperatures. ON Semiconductor has extensive experience in applications for the automotive and industrial market. Combined with the results of E^{2}COGaN it plans to use this extensive experience to expand its product lines with new applications, extending or supplanting existing HV/VHV silicon devices. The outcome of the E^{2}COGaN project will provide ON semiconductor with the knowledge and competences to provide its customers new products with increased efficiency and extended operating ranges which will directly translate to a significant reduction in cost and size of its products. Through its dedicated efforts in the field of GaN-on-Si ON Semiconductor plans to penetrate the market by 2016 with a limited market share. The plan is to increase that market share to 3% worldwide by 2018.
ST-I	STMicroelectronics has a strategic commitment in Power Conversion with its leading position. The Company portfolio completion can bring immediate benefits from E^{2}COGaN program to all ST customers and their applications' final users. More specifically, ST focus on compound semiconductor will permit ST to enforce his current and future position in the strategic market of Power Devices taking advantage from all benefits of a complete and wide product portfolio tailored with new performances and higher efficient devices. High Power devices will be more and more required, specially to drive all new coming applications where the Power efficiency will be the new must. STMicroelectronics is fully committed to bring innovation through GaN devices because through this technology ST wants penetrate the market in the next 6-8 year time frame, with a projection by 2018 to reach an EU market share of 10% (equivalent to 170MEuros).
Semikron	Assuming a positive outcome of the E^{2}COGaN project in terms of maturity and reliability of GaN-on-Si devices and module level and validation of their potential in selected relevant applications, SEMIKRON intends to produce GaN-based power modules for solar and automotive end customers. The GaN module production can be expected if the devices have passed the qualification tests and if the GaN systems can demonstrate an overall progress in price per performance (higher output current, lower losses, smaller size etc.) compared to well-established systems on Si basis. It is absolutely clear that in the next 5-10 years the price per mm2 for GaN will be higher as for Si. Therefore the GaN advantages have to be generated on system level. Semikron wants to assemble the GaN devices with new and innovative technologies at which the operation temperature of devices can be increased at the same reliability. New driver developments for high temperature application, complete power systems designed with low inductivities which allow higher switching frequencies, lower static and dynamic losses at the same output power, smaller and lighter systems and reduced cooling effort should create the necessary system benefit for GaN devices.
CIRTEM	For CIRTEM, E^{2}COGaN project will allow the validation of our driver, packaging layout and advanced isolated PFC converter with GaN devices. CIRTEM want to complete his offer on EV market with a "high performance on-board battery charger"

	(Power input: 3KW, PF>0.98, Mass<3KG, Eff>0.97) thanks to the game changing GaN power device technology. The knowledge can be applied to other products like embedded DC/DC converters and traction inverter.
EPIGAN	Expand the product range of EpiGaN towards higher voltage (2kV) and epitaxy wafers with lower sheet resistance (Rs< 250Ohm/sq;) to address new applications in automotive sector and solar converters.
CISC	The project results will be used as part of the product AT LIB and within CISC's commercial tool SyAD for system simulation
NANO	Achieved results of the E^{2}COGaN project will be applied in future research activities and other scientific projects on GaN and SiC devices, and in the field of organic electron devices. UIS multipulse test method will be optimized with focus on temperature measurements and will be finalized as automatic reliability characterization test station with utility in wide practice in further research and commercial activities.
EADS	For EADS France Innovation Works, the aim of this project is to study the capability of GaN on Si power switches to fulfil the performance and safety requirements of future more electrical aircrafts. There is especially a need for power devices able to withstand high temperature conditions with two aims: (1) Optimize the size of the required cooling system to gain on weight (2) Use power electronics to replace hydraulic parts in high temperatures areas The electrical performance, thermal capabilities and targeted cost of GaN on Si power devices make this technology be of interest for future power electronic developments in more electrical aircrafts. More especially, reliability assessment of this new technology is a key element for EADS, to assure dependability of the future electronic system based on GaN devices, especially for aircraft applications. That's the reason why EADS plans to focus his contribution on reliability domains, by making available his expertise in this field.
MC2 Technologies	For MC2 technologies this project will provide the platform for developing several equipments allowing characterization of advanced Power GaN Technologies. The project will permit to accelerate the working relationship between the major European actors and MC2 Technologies.
IUNET	Exploitations for IUNET imply the inclusion of the main concepts, objectives and results of the project in the content of a tutorial session at the end of the activity. The tutorial will focus on: - New characterization procedures for power GaN based devices; - Identification on new degradation modes and mechanisms in Power GaN devices - Simulations tools for GaN power devices (Electro-thermal and drift Diffusion) - Parasitic effects in GaN power devices.
CEA LETI	For CEA LETI, the E^{2}COGaN project will provide the platform for bringing together many advanced Power GaN Technologies. The project will accelerate the working relationship between the major European actors in the field and strengthen their overall competitive position.
FHG	The Fraunhofer Society is a leading center for applied and contract research in Germany and Europe. Therefore project results will be exploited in direct industry cooperation, where the generated know-how will be made accessible to the public to support leading innovations. Fraunhofer IZM is a centre for highly robust technologies used for system integration. A main part of the past work has been focussed on

	power electronic packaging. The project will broaden the range of knowledge to integration of GaN devices and integrating them to complete systems with enhanced operating temperatures. The gained knowledge on technologies, reliability and models will put the institute in the position to adapt project results to a range of other application conditions. This will be offered as R&D services following the general terms of the Fraunhofer Society. Fraunhofer IMS runs its own 200mm CMOS production line and has a strong focus in the high temperature electronics field. Currently customers in this field mainly come from low volume and high price markets like oil and gas drilling industry. The results of this project will enable IMS to enter the field of power electronics and energy saving with this high temperature electronics. This is a very promising market due to the emergence of very efficient power device technologies (GaN, SiC) which are capable of operation at temperatures beyond standard CMOS circuits. The availability of high temperature electronics enables smaller systems, increased reliability and less cooling efforts. By the project, Fraunhofer IISB can strengthen its position as leading R&D institution in the field of power electronics. Its competences in field of material analysis and in the functionality and reliability of Si and SiC power electronic devices are extended to GaN-on-Si topic. This will help to initiate partnerships with new industrial customers along the manufacturing chain of GaN-on-Si material producers, device manufacturers and system providers. The project tasks of IISB support the fast and cost-efficient development of epitaxy and device technology of these industrial customers and other research institutions with respect to reliability issues. Solving these problems will support the further commercialization of GaN-on-Si.
UNIVBRIS	Thermal analysis results and simulations will be fed back to the key partners in the project for the device and module developments. New thermal analysis technique developments that may emerge from the Bristol developments will be patented, subject to agreements within the consortium.
SNPS	During the last phase of the project Synopsys will enable the direct transfer of technology to the end-user of the project by providing new simulation methodologies and models in the format of TCAD simulation setups for direct industrial use. Also, the project results will be made commercially available to the industry but also to research and academia world-wide via Synopsys.
BIT	The market of of converters for EVs and HEVs is an opportunity, for Bitron, to strengthen its position in high added-value products and fully exploit its proprietary technologies for the large scale production of mechatronic systems, which have been developed and continuously improved since its foundation (1955). Its client portfolio ranging from automotive to industrial, energy and appliances, the E^2COGaN project is offering the following opportunities: • a new market with immediate chances for low-cost mass production of high efficient power electronic systems products in the order of several thousands of units/year • a partnership with GaN-on-Si suppliers to offer an integrated high-efficiency solution able to tackle the market with cost-aggressive high-added-value products
SE	Schneider Electric is looking for new power devices technologies as GaN devices for improving the efficiency of power converters and /or increasing

	the switching frequency in order to reduce the passives component size and the overall system cost. The main industrial products where these devices will be used are Motor drive, Solar inverter and Uninterruptible Power supplies (UPS)
BOSCH	Bosch as one of the largest tier 1 supplier in automotive industries focuses on wide-band-gap as fast switching, high efficiency power device solution in electric powertrains. Otherwise the field of photovoltaic power conversion is addressed by the Bosch Power Tec enterprise as well. For both fields of applications product market entry can only be realised by electronics manufactured with high quality joining and assembly processes and implemented highly robust technologies. The base for these products will be given by this activity.
TU/e	For the TU/e, this E^{2}COGaN project allows to investigate switched-capacitor circuit topologies that are especially advantageous for very high ambient temperature environments (automotive, lighting, solar, dc grid), or situations where no magnetic materials are allowed (MRI scanners). These new circuits are only feasible with the high-temperature, very fast, and low Ohmic switches made possible by GaN technology. The gained knowledge will be applied in currently running and proposed future projects with lighting, healthcare, and semiconductor equipment manufacturing companies.
AUDI	Audi wants to gain experience with GaN from device to system level. As GaN is currently not used in automotive power applications it is essential to understand the chances and limits of GaN. As for a car maker only a working system is of interest Audi wants to research what is needed to utilize the specifications of GaN successfully in robust real world applications – compared to todays solutions. GaN has the potential to enable new functions, weight reductions and thus a CO_2 reduction. Grown on silicon even the cost outlook is promising.
AZZURRO	AZZURRO Semiconductors AG as technology leader on the epitaxy of GaN on Si-Substrates will expand the portfolio for products from 150mm to 200mm with higher breakdown voltage, lower sheet resistance and e-mode designs for future commercial applications in the high power electronic market in the framework of this project.

7.3 Contribution to standards and regulations

The GaN power devices developed in the E^{2}COGaN project will have better performances in terms of electric losses compared to incumbent silicon devices used in the electronic converters, while more cost-attractive than the rivalling SiC technology. Within the E^{2}COGaN project, the benefit of the GaN power devices will be assessed on application level, focusing on selected target applications in photovoltaic and automotive. Nevertheless, the foreseen current and voltage range of these devices cover a by far larger field of appliances going from electronics converters in cars, computers, communications, industrial production processes, domestic appliances, consumer electronics, office equipment, medical engineering, energy technology, as well as to transport and traffic engineering. Power converters transform electrical energy as efficient as possible and also give the possibility to the user to control the flow of power accordingly. As a consequence, thanks to these devices the electronic equipments will be more efficient and in that terms will contribute to the European objectives as set for the reduction of energy consumption and CO_2 emission.

The reduction by 20% to 2020 of energy consumption is one of the major objectives stated by the European Commission. During the past years, the European Union has laid a corresponding legal foundation for this reduction with appropriate resolutions and directives. The “Energy Efficiency Green Paper”, the EU Directives concerning “Energy End-use Efficiency and Energy Services” and “Ecodesign Requirements for Energy-using Products”, and not least, the EU “Action Plan for Energy Efficiency” of 19- 10-2006 may be mentioned at this point.

The low power consumption by office equipment is also encouraged by the voluntary "Energy Star" energy efficiency programme adopted jointly with the United States. This promotes the manufacturing of energy-efficient office equipment. The Energy Star label enables consumers to identify low energy consumption appliances which play a part in ensuring security of energy supply and environmental protection.

In this way, the European commission is encouraging the development and investment in energy efficient products by the industry by introducing energy labels helping consumers choosing products which save energy and money. The energy labels are proposed for TVs, refrigerators, dishwashers and washing machines. The devices developed in the project are also suited for these applications and will contribute to the improvement of their efficiency.

For example the consumption of televisions, which represent almost 10% of the average household's electricity bill, it will be the first time ever that manufacturers will have to declare the energy efficiency of their products, using an A to G scale. In this way, new technologies as better performing power devices would enable to reduce the energy consumption of many electronics products. The appliances covered by the regulations adopted today represent one third of a household's electricity bill a year. The new labels will therefore have a positive impact on consumers' household expenses.

Over the duration of the project, the consortium does not plan to actively invest in standards specifically related to the field of GaN-on-Si device, modules and applications. The consortium, however, is of the opinion that the work performed in the E^2COGaN project should at least be in line with the current standards that are in place for silicon devices. E.g. the consortium is of the opinion that the research into the reliability and lifetime of the GaN-on-Si devices should meet the requirements set out in the existing standards for reliability and lifetime of silicon devices. The E^2COGaN consortium is also of the opinion that in the aftermath of this project, dedicated standards should be developed for GaN devices for power applications and that specific data investigated in this project can be used to set up these standards.

7.4 Management of intellectual property

The procedures, rules and regulations related to the management of knowledge and intellectual property will be included in the Consortium Agreement. This agreement will be signed by all consortium partners within 6 months of the project start date. The general idea behind the Consortium Agreement will be to advance the state of the art by mutual collaboration between the partners without infringing on each other’s business interests. The Consortium Agreement will describe in detail the exact ownership, subsequent exploitation of the intellectual property and dissemination and publication of the project results. The management of the intellectual property and knowledge will be performed by the coordinator in close cooperation with the various work package leaders.

In the frame of the E2COGaN project, the IPR-related activities will cover various kinds of “knowledge and invention protection” and intellectual property rights management with the objective of enhancing the exploitation of the existing and newly generated intellectual property. In order to achieve the above, specific actions will be taken to enable the creation of a project-level IPR management strategy, which will leverage the experience and

competence that is available by the partners in the consortium. Since the consortium spans partners covering the whole value chain from substrate providers, GaN device manufacturers, assembly houses to end users, there will be a multitude of opportunities by the partners in the consortium to create valuable IP. The consortium, however, does see clear opportunities for the semiconductor manufacturers for the creation of IP during the device development and on the assembly and system side.

8 QUALITY OF CONSORTIUM AND MANAGEMENT

8.1 Management structure and procedures

In order to achieve the objectives of the project and to contribute to the overall success of the project it is imperative that a well-defined organizational structure is in place. This organizational structure will take into account all aspects of the project ranging from management of technical activities and coordination of the integration of the various work packages to quality control, financial control, legal and administrative control, and communication within the project and towards the European Commission.

The proposed management structure is not a novelty in itself, but it builds upon the management structure and procedures of former and ongoing successful EU-funded projects of similar size and impact (ENIAC SmartPM, ENIAC END, ENIAC E3Car, ENIAC ERG, ENIAC E2SG, ENIAC Cajal4U, FP7 SMAC, FP7 Pullnano). The management structure and procedures of the above mentioned projects have proven to be adequate, efficient and more than capable to respond to any changes and threats to the project.

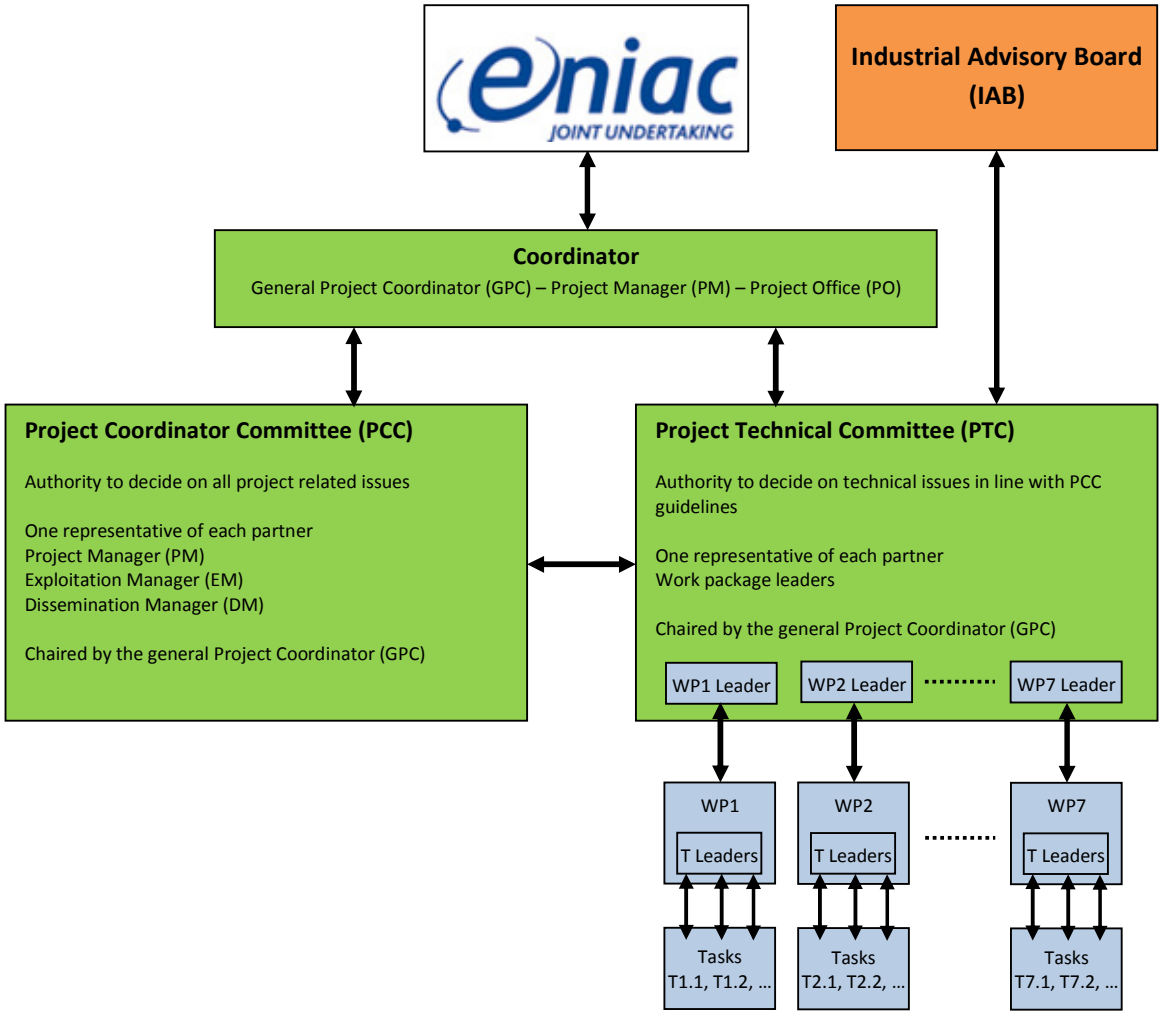

Figure 18: Project Management Structure

Hence, to guarantee a flawless execution of the project, the following management structure and functions will be put in place:

- General Project Coordinator (GPC),
- Project Coordinator Committee (PCC),
- Project Technical Committee (PTC),
- Project Manager (PM),
- Exploitation Manager (EM),
- Dissemination Manager (DM),
- Work Package Leaders (WPLs),
- Task leaders (TLs),
- Project Office (PO),
- Industrial Advisory Board (IAB).

The interactions between the various functions are depicted more in detail in Figure 18.

With the above displayed management structure in mind, the project is coordinated by the General Project Coordinator. The Project Coordinator Committee decides on all project-related issues. The Project Technical Committee, however, decides on all technical project-related issues. The PTC will also function as the main interface to the Industrial Advisory Board. Both PCC and PTC are assisted by the Project Office, which is located at the Project Coordinator site. Each work package in the project will be coordinated by the corresponding Work Package Leader, while each task in the various work packages will be coordinated by the corresponding Task Leader.

8.1.1 General Project coordinator (GPC)

The project will be coordinated by the General Project Coordinator, who will be assisted by the Project Office. The GPC is responsible for the following tasks:

- Interfacing to the ENIAC JU,
- Preparation of reviews and project meetings (PCC, PTC),
- Chairing of the PCC and the PTC,
- Negotiating of contract, budget, consortium agreement, etc.,
- Representing the consortium,
- Day-to-day management of the consortium which includes but are not limited to monitoring of the project progress and resource usage, anticipating corrective actions when necessary, resolve conflicts within the consortium when they arise, etc.

8.1.2 Project Coordination Committee (PCC)

The PCC shall be composed of one representative of each partner in the consortium, the GPC, the PM, the DM and the EM. Each representative will have the authority to make decision on behalf of the organization he/she represents in terms of overall strategy and resources allocated to the project. The GPC will chair the PCC. The PCC is responsible for the overall direction of the project and has final decision authority. The PCC will meet at least twice per year and more often if deemed necessary for administrative and scientific management. The decisions will be taken by consensus or by simple majority in the case where a consensus cannot be reached. Changes to the work-plan will require consensus or a double majority. Each member of the PCC will have one vote. The General Project Coordinator will resolve any tie in the vote. The voting procedure as well as the responsibilities of the PCC will be described in detail in the Consortium Agreement. The main responsibilities of the PCC are the following:

- The management of the project,
- Deciding on possible changes to the work-plan,

- Approving on the (re) allocation of the project's budget,
- Making proposals for reviewing/amending the contract, if the need arises,
- Proper handling of defaulting partners,
- Deciding on issues like technical roadmaps, joint publications and press releases, IP rights, exploitation and dissemination plans, control and auditing procedures,
- Maintaining the consortium agreement,
- Appointing the exploitation and dissemination manager.

8.1.3 Project Technical Committee (PTC)

The PTC is composed of the WP Leaders and, since all partners in the Consortium shall be represented in the PTC, (co-opted) partner representatives, plus the GPC, the PM, the EM and the DM. Members of the PTC differ from the PCC for their scientific and technical focus. The representative in the PTC shall be able to make decisions as to the particular technical interests and how to use the resources allocated to achieve the project's objectives. The members of the PTC will be appointed by each of the prime partners. The GPC will chair the PTC. The PTC is responsible for the monitoring of the project progress and the preparation, review and updating of the detailed work-plan. The decisions will be taken by consensus or by a simple majority in the case where consensus cannot be reached. Each member of the PTC will have one vote. Changes to the work-plan will require consensus or a double majority. The PTC will meet every 2 months. Meetings will be generally held by telephone conference. The voting procedure as well as the responsibilities of the PTC will be described in detail in the Consortium Agreement. The main responsibilities are summarized as:

- Coordinating the overall technical work on a continuous basis,
- Coordinate the interaction and collaboration across Activities,
- Preparing proposals for the PCC on issues like the (re) allocation of budget, the adaptation of the work-plan, whenever the need arises.

8.1.4 Project Manager (PM)

The project manager is appointed by the Project coordinator. He/she is the head of the Project Office and is in charge of the daily management of the project activities.

8.1.5 Exploitation Manager (EM)

The Exploitation Manager will be responsible for the day-to-day management of the exploitation activities within the project. The Exploitation Manager will be in charge of the coordination of the exploitation activities for the E^2COGaN consortium as a whole. The Exploitation Manager is a voting member of the PCC and the PTC, and is appointed by the PCC.

8.1.6 Dissemination Manager (DM)

The Dissemination Manager will be responsible for the day-to-day management of the dissemination activities within the project. The Dissemination Manager will be in charge of the coordination of the dissemination activities for the E^2COGaN consortium as a whole. The Dissemination Manager is a voting member of the PCC and the PTC, and is appointed by the PCC.

8.1.7 Work Package Leader

The main responsibilities of the WP Leaders are the following:

- Coordinate the work in the various work packages,

- Ensure a close communication among the participants
- Convene the work package internal meetings,
- Ensure the on-time delivery of work package deliverables,
- Participate to the meetings of the PTC,
- Report progress and deviations from the work-plan to the GPC and the PTC.

Work package Leaders are assisted by Task Leaders, whose responsibility is to:

- Organize the technical exchanges between the partners contributing to the Task,
- Check the progress and on-time delivery of the Deliverables of the Task,
- Report to the Work Package leader, who will be coordinating all Tasks of the respective work package.

8.1.8 Project Office

The major responsibility of the Project Office will be administrative management and support. The Project Office is located at the coordinator's site and the main responsibilities include but are not limited to the following:

- Organizing meetings of members of the consortium,
- Collecting documentation for the monitoring of activities within the various work packages,
- Collecting deliverables for submission to ENIAC JU,
- Preparing detailed list on deliverables and milestones, partner contact information, management and updating of the project calendar, establishing mailing lists, etc.

8.1.9 Industrial Advisory Board (IAB)

An industrial panel representing major end users not participating to the E^2COGaN project will be established within 3 months of the project start. The panel will be established under the shared responsibility of the Dissemination and Exploitation Managers with the support from all partners in the consortium. On regular basis, the panel will be informed about the progress of the project. In return, the panel will be asked to guide and advise the consortium on technical and strategic matters for achieving the project objectives. The panel will be requested to advise the consortium on the following:

- Specifications and requirements related to WP1 according to their specific know-how and business interest,
- Provide technical and strategic advice regarding R&D work performed in WP2, WP3 and WP4,
- Contribute where possible to the dissemination activities of WP6,
- Participate where possible to the exploitation of the project results.

8.1.10 Management procedures

At the start of the project, a set of management procedures will be put in place that ensure proper handling of the following activities:

- Decision making and communication handling,
- Management concerns,
- Escalation procedures,
- Progress monitoring,
- Corrective actions, and
- Quality assurance.

8.2 Individual partners

The following tables contain detailed description of the contributing partners, a reminder of their main duties on the project, the expertise they bring in and short resumés of the key personnel involved in E²COGaN.

(1) ON Semiconductor Belgium BVBA (ONsemi)

Description of the Legal Entity:

With its global logistics network and strong product portfolio, ON Semiconductor is a preferred supplier of high performance, energy efficient, silicon solutions to customers in the power supply, automotive, communication, computer, consumer, medical, industrial, mobile phone, and military/aerospace markets. The company's broad portfolio includes power, analogue, DSP, mixed-signal, advance logic, clock management, non-volatile memory and standard component devices. Global corporate headquarters are located in Phoenix, Arizona, U.S. The company operates a network of manufacturing facilities, sales offices and design centers in key markets throughout North America, Europe, the Asia Pacific regions and the Middle East. On Semiconductor has a strong presence in Europe.

Main Tasks within E²COGaN:

- WP1: Translation of application needs into technical device requirements
- WP2: conception, layout, optimization, manufacturing and characterization of GaN power devices (Schottky diodes and (MIS)HEMTs)
- WP3: Robustness and reliability assessment and improvement of GaN power devices enabling further use in WP4 and WP5
- WP4: Provision of GaN power devices
- WP5: Provision of GaN power devices (Battery Charger)
- WP7: Overall project management

Profile and Expertise: ONSemiconductor Belgium comprises manufacturing facilities and design centres. A large R&D effort is dedicated to analogue and high voltage devices, process technology and reliability, innovative design and test techniques and new circuit concepts. Engineers from On Semiconductor in Belgium have co-operated with many European partners in the frame of IST, ENIAC, ARTEMIS and MEDEA+/ CATRENE projects.

CV of Staff scientists involved:

Dr. Peter Moens received a M.Sc. and a Ph.D. in solid state physics from the University of Gent, Belgium, in 1990 and 1993 respectively. From 1993 till 1996, he worked as a post-doctoral fellow in collaboration with Agfa-Gevaert, Mortsel Belgium on the electron capture efficiency of silver halide emulsions. In 1996, he joined ON Semiconductor, Oudenaarde, Belgium where he was involved in the technology and device development for smart power applications, and the related reliability aspects. Since 2008 he is responsible for the development of 600+V discrete power devices, both in silicon as well as in wide band gap materials. He is author or co-author of over 120 papers in international scientific journals and in international conference proceedings, and has issued over 15 patents in his field of application. Dr. Moens is member of the technical program committee of ISPSD, IRPS, IRW, ESREF and the ESD/EOS Symposium, and served as the chair of the HV reliability subcommittee of IRPS. He also served as the technical program chair of ISPSD2009, and will be the general chair of ISPSD2012. He is Guest Editor of IEEE Transactions on Devices and Material Reliability.

Frederik Deleu received the MASc. degree in electrical engineering from Dalhousie University, Halifax, Canada in 2004. In 1998 he joined ON Semiconductor Belgium (then Alcatel Microelectronics). Between 1998 and 2006 he has held the position of Modeling Engineer in ON Semiconductor's Belgium and Taiwan offices. From 2006 until 2010 he managed ON Semiconductor's US modeling department. He is currently manager of R&D programs in the corporate R&D department and focuses mainly on smart power technologies, applications and circuits.

(2) NXP Semiconductors Netherlands BV (NXP-NL)

Description of the Legal Entity:

NXP Semiconductors had been founded by 2006 out of a former division of Philips. NXP Semiconductors provides High Performance Mixed Signal and Standard Product solutions that leverage its leading RF, Analog, Power Management, Interface, Security and Digital Processing expertise. These innovations are used in a wide range of automotive, identification, wireless infrastructure, lighting, industrial, mobile, consumer and computing applications. A global semiconductor company with operations in more than 25 countries, NXP posted revenue of $4.2 billion in 2011. Headquartered in Europe, the company has around 23,000 employees working in 20 countries across the world.

Main Tasks within E^{2}COGaN:

- WP1: Translation of application needs into technical device requirements
- WP2: Conception, layout, optimization and characterization of GaN power devices (Schottky diodes and HEMTs)
- WP3: Robustness and reliability assessment and improvement of GaN power devices enabling further use in WP4 and WP5

Profile and Expertise:

NXP Semiconductors NL brings in its Central R&D facility located at Eindhoven, home of about 250 employees. Concerning the Process Technology Sector, its expertise lies in semiconductor process technology (including GaN), active and passive device simulation, design and characterization. Moreover, NXP Central R&D NL has a strong design and application-oriented research activity.

CV of Staff scientists involved:

Dr. Jeroen A. Croon was born in Delft, The Netherlands, in 1975. In 1998, he received the Master's degree in applied physics from the Delft University of Technology. After this, he started working in IMEC, Belgium, and in 2004 he received the Ph.D. degree in electrical engineering from the Catholic University of Leuven, Belgium, for his study of the matching properties of deep-submicron MOSFETs. After obtaining his Ph.D. he worked in IMEC on the characterization of MOSFETs fabricated on germanium substrates and on the study of variability in advanced CMOS processes. Since the beginning of 2005, he has been working in the compact modeling group of NXP Semiconductors Research, Eindhoven, The Netherlands, on the modeling of RF circuit blocks. Since 2011 he started working on characterization of GaN power switches.

(3) NXP Semiconductors UK Ltd. (NXP-UK)

Description of the Legal Entity:

NXP Semiconductors had been founded by 2006 out of a former division of Philips. NXP Semiconductors provides High Performance Mixed Signal and Standard Product solutions that leverage its leading RF, Analog, Power Management, Interface, Security and Digital Processing expertise. These innovations are used in a wide range of automotive, identification, wireless infrastructure, lighting, industrial, mobile, consumer and computing applications. A global semiconductor company with operations in more than 25 countries, NXP posted revenue of $4.2 billion in 2011. Headquartered in Europe, the company has around 23,000 employees working in 20 countries across the world.

Main Tasks within E^{2}COGaN:

- WP1: Translation of application needs into technical device requirements
- WP2: GaN Process Development and GaN Device Manufacturing
- WP4: Delivery of GaN power devices
- WP5: Delivery of GaN power devices (PV string inverter)

Profile and Expertise:

The site based in Hazel Grove near Manchester employs over 400 people and is home to the PowerMOS business unit, which has a large R&D group, Marketing and Sales and a 6" Silicon wafer fabrication facility, with a track record for designing and manufacturing power MOSFET devices since the 1970s and currently produces over 530 million devices a year. For the past 15 years it has been developing its TrenchMOS family of devices and has recently released the 7th generation of the technology, establishing itself as a leading supplier to the power electronics industry and is ranked the market leader in low-voltage MOS for automotive applications, winning many awards including Bosch's 2011 Best Supplier Award in the 'Electronics and Electromechanical Components' category. The site is also the primary production facility for the development of products in GaN-on-Si for the High-Voltage power applications.

CV of Staff scientists involved:

Andrew Rimmington has a B.Eng in Electrical and Electronic Engineering from Nottingham Trent University with over 24 years of experience in the semiconductor industry. He has managed global organizations developing complex System-on-Chip (SoC) and IP projects supporting programs in GSM, 3G, Bluetooth wireless markets and the development and introduction of the a 45nm Advanced CMOS technology platform for development of products in Set-Top-Box and LCD TV applications, currently he is the program manager responsible for the development and industrialization of NXPs first generation GaN-on-Si technology for power applications to be deployed in Manchester.

Dr. Mark Gajda received his PhD from the University of Cambridge in 1994 in the field of microelectronics. Since then he has been engaged in the development of power transistors, working for Philips and NXP Semiconductors. He has been instrumental in the development of several generations of power MOSFETs and has extensive experience and knowledge of the development cycle, from concept to industrialisation. He is the co-author of several publications and has issued several patents in the field of power semiconductors. He has additional relevant experience in project management, TCAD modelling, packaging, multi-site platform development and product qualification.

(4) NXP Semiconductors Belgium NV (NXP-B)

Description of the Legal Entity:

NXP Semiconductors had been founded by 2006 out of a former division of Philips. NXP Semiconductors provides High Performance Mixed Signal and Standard Product solutions that leverage its leading RF, Analog, Power Management, Interface, Security and Digital Processing expertise. These innovations are used in a wide range of automotive, identification, wireless infrastructure, lighting, industrial, mobile, consumer and computing applications. A global semiconductor company with operations in more than 25 countries, NXP posted revenue of $4.2 billion in 2011. Headquartered in Europe, the company has around 23,000 employees working in 20 countries across the world.

Main Tasks within E^{2}COGaN:

- WP1: Translation of application needs into technical device requirements
- WP2: Work package leader, conception, layout, optimization and characterization of GaN power devices (Schottky diodes and HEMTs)
- WP3: Robustness and reliability assessment and improvement of GaN power devices enabling further use in WP4 and WP5

Profile and Expertise:

NXP Semiconductors Belgium brings in its Central R&D entity located at Leuven, home of about 30 employees as a satellite of the Central R&D activities of Eindhoven (NL). Its expertise lies in semiconductor process technology (including GaN), active and passive device simulation, design and characterization with a strong focus on HV devices. NXP Semiconductors Belgium has been or is involved in numerous European Projects (FP7, ENIAC, etc.), such as PullNANO and CAJAL4EU.

CV of Staff scientists involved:

Dr. Markus Müller is senior scientist at NXP Research in Leuven. He received his MASc in solid state physics 1997 at the University Joseph Fourier of Grenoble. After his PhD in physics on II-VI semiconductor optics - obtained in 2000 at the CEA in Grenoble (F) - he worked seven years as a research engineer for Philips/NXP on CMOS scaling (65 to 32nm nodes) within the Crolles2 Alliance between Freescale, STMicroelectronics and Philips/NXP. In 2007 he joined NXP Research Belgium to lead the 22nm High-K / metal gate integration project before joining 2009 the high voltage and GaN team where he is focusing on device physics. He was actively involved as technical contributor and work package leader in the FP6 European projects NanoCMOS and Pullnano, the latter having received an excellence award for its outstanding achievements. Author of more than 30 publications and inventor of numerous patents he was member of the European technical committee of The VLSI Technology Conference from 2008-2011.

(5) STMicroelectronics Italy (ST-I)

Description of the Legal Entity:

STMicroelectronics is one of the world's largest semiconductor companies with net revenues of US$ 9.73 billion in 2011. Offering one of the industry's broadest product portfolios, ST serves customers across the spectrum of electronics applications with innovative semiconductor solutions by leveraging its vast array of technologies, design

expertise and combination of intellectual property portfolio, strategic partnerships and manufacturing strength. The Company has particular strengths in Multimedia, Power, Connectivity and Sensing technologies and its sales - which includes wireless business conducted via ST-Ericsson, the 50/50 Joint Venture with Ericsson, - are well balanced among the industry's major sectors: Telecom (30%), Automotive (18%), Consumer (10%), Computer (13%), Industrial (9%) and Distribution (20%).

Main Tasks within E^{2}COGaN:

- WP1: : Translation of application needs into technical device requirements
- WP2: Manufacturing of GaN HEMT CMOS compatible at 6"(HV) and "(LV)
- WP3: Robustness and reliability assessment and improvement of GaN power devices
- WP4: Design manufacturing and characterization of IC's driver
- WP5: Implementation and Evaluation of micro-inverter demonstrator

Profile and Expertise:

Since its creation, ST has maintained an unwavering commitment to R&D and is one of the industry's most innovative companies. In 2011 the Company spent about 24% of its revenue in R&D. Among the industry's most innovative companies, ST owns over 21,500 patents and pending patent applications. ST's process technology portfolio includes advanced CMOS (Complementary Metal Oxide Semiconductor) logic including embedded memory variants, mixed-signal, analog and power processes. ST has a worldwide network of front-end (wafer fabrication) and back-end (assembly and test and packaging) plants.

ST has established a worldwide network of strategic alliances, including product development with key customers, technology development with customers and other semiconductor manufacturers, and equipment- and CAD-development alliances with major suppliers. These industrial partnerships are complemented by a wide range of research programs conducted with leading universities and research institutes around the world, in addition to playing a key role in Europe's advanced technology research programs such as CATRENE (Cluster for Application and Technology Research in Europe on NanoElectronics), a successor to MEDEA+, and industry initiatives such as ENIAC (European Nanoelectronics Initiative) and ARTEMIS (Embedded Computing Systems Initiative).

ST(I) based in Italy manufacturing and design centers dedicating large efforts to analog and power devices. In the field of semiconductors compound a production and development line for SiC and GaN is based in Catania.

CV of Staff scientists involved:

Dr. Alfonso Patti graduated in Physic with full marks at Catania University in 1977. In 1979 he joined ST as power bipolar designer becoming design manager in 1985. He enriched his expertise on power switch from 1986 for ten years managing design activity for power bipolar, powerMOS and RF power. During year 2000 he joined R&D department as manager for RF technology and design. On top of this activity he started the GaN technology development inside the Industrial multi-segment sector R&D, where today he is director for RF and GaN technology. He published articles on international scientific magazine and he is owner of international patents.

Dr. Francesco Gennaro graduated in 1996 and pursued the Ph.D. degree in 2000 both in Electrical Engineering at the University of Catania (Italy). In 1999 joined the University of Wisconsin, Madison-WI-USA as Visiting Scholar and worked as New Product Development

Engineer at “Soft Switching Technologies Corporation”, Madison-WI-USA. In 1999-2000 was Associate Researcher at the Department of Electrical and Electronic Engineering of the University of Catania and then joined STMicroelectronics as Senior Application Engineer for High Voltage Smart Power ICs. Currently he is “Power Converter Team Manager” in IMS Systems Lab and Technical Marketing in STMicroelectronics, Catania (Italy). Dr. Gennaro is a Technical Staff Member inside STMicroelectronics with major expertise on power conversion in high efficiency applications and renewable energy. He is the Project Coordinator in “ENIAC ERG” project and is Work Package leader in other European and National Funded Projects in energy efficiency and renewable energy segments. He is author of more than 35 scientific papers and holds 5 international patents on Power Conversion. His main interests are low power AC-DC and DC/DC converters, renewable energy electronic power converters, system integration and electromagnetic compatibility (EMC) in power electronics.

Dr. Cateno Marco CAMALLERI was born in 1967 and has a degree in Physics (Biophysics) in 1992 at the Palermo’s University. In 1993 he joined ST Microelectronics Catania R&D. Starting from diffusion process area he worked as process integrator for power silicon devices, power compound semiconductors devices, photovoltaic systems, plastic electronics. He is coauthor in several scientific papers and patents. Today he is in charge for Compound Semiconductor Process Integration Group within the IMS R&D Technology Development Group.

Dr. Marco Morelli was born in Livorno, Italy, in 1950. He received the degree in electronic engineering from the University of Pisa. Since 1979 in STMicroelectronics he has been for several years responsible for analogue and mixed mode ICs dedicated to the automotive field. Nowadays is responsible in the research department for the development of advanced projects achieved with not conventional silicon technologies. He is co-author in 34 industrial patents.

(6) Semikron Elektronik GmbH & Co KG (Semikron)

Description of the Legal Entity:

Semikron is an internationally leading power semiconductor manufacturer. Founded in 1951, the German-based family enterprise employs 3200 people worldwide. Semikron comprises a global network of 35 companies with production plants in Germany, France, Italy, Slovakia, Brazil, USA, China and India.

The products range from power device chips (wafer fabrication), discrete semiconductor, MOSFET-, IGBT- diode- and thyristor modules (different assembly lines with different technologies) to customer specific solutions and integrated power electronic systems (system assembly) for applications from one kilowatt into the Megawatt range. The main application fields are industrial drives, power supplies, electric vehicles, rail drives and renewable energy (wind, photo voltaic). Semikron is the market leader in the field of diode/thyristor modules, enjoying a 37% share of the worldwide market. Semikron technology powers nearly the half of the globally installed wind power capacity with IGBT used integrated power systems.

Main Tasks within E^{2}COGaN:

- WP4 : conception, design, implementation and evaluation of power modules (using advanced die attach and bonding solutions) and gate drivers; provision of power modules and gate driver for inverter for WP5

Profile and Expertise:

As a significant innovator in the power electronics sector, many of Semikron´s progressive developments have been accepted as industrial standards. Over 100 development engineers work in the field of power semiconductor development, module-, driver- and system-design and power electronic application.

CV of Staff scientists involved:

Dr. Reinhard Herzer is the technical representative of Semikron Germany E^{2}COGaN project on packaging, IC-and system design and validation.

He studied Electrical Engineering and received 1984 his PhD in the field of Microelectronics and 1992 his Habilitation in the field of Power Devices and Smart Power ICs from the Technical University of Ilmenau. He joined Semikron Electronics Nuremberg, Germany in 1995 as head of the MOSFET, IGBT and IC research department. Here he is responsible for the introduction of new power device generations as well as driver- and sensor- IC in new power modules and systems.

Further he is Associated Professor at the Technical University of Ilmenau where he teaches and coaches students and PhD students. He is holder of several patents regarding power devices and driver-IC, and has published over hundred of papers and conference contributions respectively.

(7) CENTRE D'INGENIERIE ET DE RECHERCHE DES TECHNOLOGIES DE L'ELECTROTECHNIQUE MODERNE (CIRTEM)

Description of the Legal Entity:

CIRTEM was founded in 1988, on the fringe between research laboratories and industry. This independent company quickly became a vector for technological transfer in power electronics. CIRTEM imagine, develop, industrialize and commercialize new technologies of switching power conversion. CIRTEM innovation service has a staff of 16 people (5 Doctors, 3 Engineers, 4 Technicians) located in Labège-Innopole near Toulouse and 1 Doctor in PRIMES platform in Tarbes, while CIRTEM products service is located in Ste Foy d'Aigrefeuille with a staff of 14 people (5 Eng., 6 Tech., 3 Work.). CIRTEM has the status of "Contracted Research Company" (SRC) since 1991. CIRTEM created and validated innovative technologies for high frequency power conversion in varied field (automotive, aircraft, military, railway infrastructure, industrial equipments). In 2005, CIRTEM provided 440 High Precision and High Frequency Four-Quadrant Power Converter (+/-10V +/-600A) for the CERN LHC. Since 2007, CIRTEM provides power converters for Military Sonar to Thales Underwater Systems. In 2011, CIRTEM began producing the traction inverter for the BLUECAR (AUTOLIB). 2011 revenues was 3.8M€ and the growth rate is about 40% per year.

Main Tasks within E^{2}COGaN:

- WP1: Provision of customer requirement specs and translation into technical requirements (battery charger demonstrator)
- WP4 : Conception, implementation and evaluation of High-frequency capable power modules and gate drivers targeting the battery charger demonstrator
- WP5: Conception, implementation and evaluation of battery charger demonstrator

Profile and Expertise:

CIRTEM innovation conduct research on SiC converters (1200V&3300V), Interleaved Parallel Converters with intercell transformers, new embedded electrical network architecture, while developing Electrical Vehicles and converters for energy storage and/or fuel cell interfacing and managing. Since 2010, CIRTEM has been involved in the SiC packaging through the platform PRIMES. With a team of over 10 specialists, CIRTEM imagine and develop new technologies of switching power conversion.

CV of Staff scientists involved:

Dr. Philippe Cussac studied Power Electronics at "Institut National Polytechnique de Toulouse". He received my Ph.D. in 1991 on "Travelling Wave Tube Power Supply". He joined CIRTEM in 1992 to work on switching power converters R&D. He is current interest is on new structures of power conversion, wide gap power components and their integration in power modules for various applications from 600V (EV) to 3.5KV (Power Systems).

(8) EpiGaN NV (EPIGAN)

Description of the Legal Entity:

EpiGaN N.V has been created in 2010 as a spin-off of imec. While its new production facility has been inaugurated in May 2012, EpiGaN is today starting production from its new site in Hasselt and is currently actively hiring and expanding. EpiGaN gives device manufacturers access to its unique, proven and powerful GaN epitaxy substrate technology for key market segments such as power supplies for consumables, hybrid electric vehicles, solar inverters, RF power for base stations, smart grid.

Main Tasks within E^{2}COGaN:

- WP2: Provision and optimization of 6' 800V wafers and conception and implementation of 6' 1500V wafers

Profile and Expertise:

EpiGaN's founders were among the pioneers to develop GaN on Si technology. While still at imec, they were the first to demonstrate GaN HEMT's on 6" and 8" Si substrates. EpiGaN also has extensive experience with growth on sapphire, SiC and native GaN substrates.

The EpiGaN team has co-authored more than 100 publications, among them several in the emerging field of GaN high voltage switching devices, demonstrating state-of-the-art results for both material and devices.

A key concept of the technology is in-situ SiN, providing excellent passivation and superior device reliability.

CV of Staff scientists involved:

Dr Marianne Germain, co-founder and CEO of EpiGaN, obtained her PhD in Electrical Engineering in 1999 from University of Liege, in a project in collaboration with RWTH Aachen. After short stays as invited post-doc engineer in Purdue University and Würzburg University, she joined imec (Leuven) in 2001. She took part in the development of Gallium Nitride growth and component technology for high power/high frequency applications. Since 2004, she was program manager of IMEC's strategic driver "Efficient Power" (GaN-on-Si). She co-founded EpiGaN in may 2010.

Dr Joff Derluyn, co-founder and CTO of EpiGaN, graduated from Ghent University in 1998 as an electrical engineer and continued to pursue a PhD degree at the same university which he obtained in 2003 on the topic of MOCVD growth of dilute nitrides. He then moved to imec where he focused on processing and device aspects of III-nitride devices, eventually becoming responsible for the III-nitride device activity. He co-founded EpiGaN in may 2010.

Dr Stefan Degroote, co-founder and COO of EpiGaN, obtained his M.Sc and PhD degrees in Nuclear Solid State Physics from the University of Leuven in 1993 and 1998. His PhD focused on the deposition and characterization of epitaxial silicides. After this, he joined imec where he became responsible for III-V Epitaxy. His current research interests are the material science and fabrication of novel III-Nitride hetero structures for electronic applications. In may 2010, he co-founded EpiGaN.

Dr Domenica Visalli, obtained her PhD from imec in 2011. Her PhD focused on the study of breakdown mechanisms in AlGaN/GaN HEMTs. She graduated from the University of Messina in 2006 as an electrical engineer, with “110/110, cum laude”. She joined EpiGaN in 2011. Her main focus is on GaN material characterization and related breakdown mechanisms.

(9) CISC Semiconductor GmbH (CISC)

Description of the Legal Entity:

CISC is a design and consulting service SME for industries developing embedded microelectronic systems with extremely short Time-To-Market cycles. CISC core competences are: System design, modeling, simulation, verification and optimization of heterogeneous embedded microelectronic systems with a particular focus on Automotive and RFID systems. CISC customers are represented in the Semiconductor, Automotive and RFID industry.

The company was founded in 1999 and is 100% private owned. CISC is managed by an international team of experts (100% master or PhD degree). The main office is in Klagenfurt, Austria with an R&D branch office in Graz, Austria. Products and services are located in three different business units: "Automotive", "RFID + RFComm" and "Tools + Methodology.

Main Tasks within E^{2}COGaN:

- WP4: Model development of components suitable for design space exploration on system level
- WP5: Existing (co-)simulation capabilities will be further developed exactly to bring the advantages of GaN technology to the system level
- WP6: Dissemination of extended simulation capabilities mapped to modules of an existing co-simulation framework.

Profile and Expertise:

CISC has ongoing research and development in the field of embedded systems with focus in Automotive and RFID/RF Communication applications. In total CISC was participating over the last 12 years with more than 60 Person years in joint European RTD projects as partner in EUREKA, EU FP and JTI projects. Currently CISC is Partner in ENIAC project e3car and ARTEMIS projects POLLUX and IoE and in CATRENE Projects SR2 and CoSIP.

CV of Staff scientists involved:

Dr. Markus Pistauer (CEO) holds a Master degree in Electrical and Electronic Engineering (1991) and a Ph.D. degree in Electronic and Control Engineering (1995), both

from Graz University of Technology, Austria. From 1995 to 1999 he worked at Siemens AG (Semiconductor Division, now Infineon Technologies) and also as Professor at University of Applied Sciences, Carinthia. He has founded CISC Semiconductor in 1999 where he acts as CEO. He gathered significant experience within a couple of national and international collaborative research projects over the past 15 years. He is author and co-author of more than 60 papers published in the field of the entire project.

(10) NanoDesign, ltd. (NANO)

Description of the Legal Entity:

NanoDesign ltd. is a spin-off company, founded in 2007 by a group of specialists in field of precise measurement in bioelectronics. A year later several experts in field of semiconductor devices characterization and testing joined the company in order to provide technological transfer in Slovakia. Today it is research and development company composed of up to 10 full-time research workers. Strong connection to university provides the company yearly with by extra 3-4 PhD students. Several research projects are being resolved yearly, mostly in field of design of precise bioelectronics measurement devices and semiconductor devices and modules testing and characterization. NanoDesign is one of a kind company within the country with orientation to research in field of semiconductor devices testing. During previous projects some high precision test stations were developed. These devices (TDR, multipulse UIS) facilitate selective research tasks in current national funded projects. Staff members actively participate at the education process and provide successful technological transfer between academia and industry

Main Tasks within E^{2}COGaN:

- WP3: multipulse UIS inductive switching, on-chip characterization and reliability assessment
- WP4: failure analysis based on electrical characteristics and SEM/EDS and spectral cathodoluminiscence measurements, dc/ac modules pulse measurements and voltage stress test

Profile and Expertise:

NanoDesign, ltd. is grouping experts in field of semiconductor structures characterization and testing together with microelectronics design engineers. Several precise test units were designed and prepared for utilization of unique off-chip and on-chip multipulse UIS measurement or scalable temperature TDR on-chip characterization. Besides this we are strong in low frequency noise analysis, failure analysis and reliability tests. Experience in field of own precise electronic test stations design help to facilitate tasks within R&D projects with orientation to technology transfer.

CV of Staff scientists involved:

Dr. Martin Daricek studied at Slovak University of Technology in Bratislava where he received his PhD degree in field of device and IC characterization. He has carried out postgraduate studies in area of IC characterization methods development. He is cofounder of spin-off company NanoDesign, ltd. with focus on off-chip innovative measuring and testing devices design and semiconductor devices characterization. Besides this is he currently responsible for R&D projects management. In present, he participates at university as a part time teacher.

Dr. Martin Donoval received his master and PhD degrees in Electronics from Slovak University of Technology in Bratislava. He has carried out postgraduate studies in area of IC design. Afterwards he continued working at the university as a research assistant in

magnetic force affected IC sensors design and magnetic force IC sensors. He participated in the establishment of the spin-off company NanoDesign with focus on reliability testing, structure characterization and off-chip innovative solutions design. Today he is responsible for R&D projects management, particularly in a field of electronics design. He participates in development of new prototypes and dedicated integrable electronics and realibility testing.

(11) EADS (EADS)

Description of the Legal Entity:

The European Aeronautic Defence and Space Company N.V. (EADS) is a global pan-European aerospace and defence corporation and a leading defence and military contractor worldwide. The group includes: Airbus as the leading manufacturer of commercial aircraft, with Airbus Military covering tanker, transport and mission aircraft; Eurocopter as the world's largest helicopter supplier; Astrium, the European leader in space programmes from Ariane to Galileo; and Cassidian as a provider of comprehensive and integral systems solutions for aerial, land, naval and civilian security applications. In 2010, EADS generated revenues of €45.75 billion and employed 121,700 personnel.

Main Tasks within E^{2}COGaN:

- WP1: Provision of specifications for Aeronautic applications and translation into technical requirements.
- WP3: Reliability and Robustness of GaN devices for Aeronautic requirements:reliability assessment of device in standard package and radiation sensitivity to Single Event Effect
- WP4: Assembly and gate driver activities: Reliability and Robustness of advanced packages and gate drivers for specific Aeronautic requirements (>200°C) Electromagnetic Compatibility studies of dies in the package.
- WP5: Evaluation of GaN-based demonstrator for Aeronautic applications to EMC requirements

Profile and Expertise:

A global network of Technical Capability Centers collectively known as EADS Innovation Works (IW) is operating the corporate Research and Technology (R&T) laboratories that guarantee the company's technical innovation potential with a focus on the long-term. Supporting all the EADS Business Units, they have the mission to identify new value-creating technologies and to develop technological skills and resources. EADS Innovation Works fosters technological excellence and business orientation through the sharing of competences and means between the various partners of the EADS Group and develops and maintains partnerships with world-famous schools, universities and research centers. EADS IW employs 600 people. More especially, EADS IW Suresne & Toulouse, France, are in charge of power electronic expertise.

CV of Staff scientists involved:

Dr. Olivier Crepel is research engineer at EADS IW in Toulouse, France, specialized in power electronics and electronic systems dependability.

He received his Master degree in Electronics, specialized in microelectronics, from the University of Lille in 2001. From 2001 to 2004, he worked at Philips/NXP Caen, in partnership with CNES Toulouse, as PhD student, developing advanced Failure analysis techniques, and then obtained his Ph.D. degree in Reliability and Failure Analysis of Integrated Circuits. In 2004, he joined Motorola/Freescale, in Toulouse, working in the

Quality organization as a Failure Analyst Engineer, then Failure Analysis Team Manager and finally Quality and Reliability team expert, specialized in mixed-mode devices for automotive applications. Author of more than 15 papers and inventor of 3 patents and several trade-secrets, he is reviewer of publications at IEEE/ Electron Devices Society and is board of directors member at the European Failure Analysis Network (EUFANET).

(12) MICROWAVE CHARACTERIZATION CENTER SAS (MC2)

Description of the Legal Entity:

MC2-Technologies is a center of characterization, modeling and design of microwave components and systems. The company was created in March 2004 as simplified public company with a registered capital of 95kEUR. MC2-Technologies is a spinoff of the Institut d'Electronique, de Microélectronique et de Nanotechnologie (IEMN)

The company presents three complementary activities in constant progress since its creation: The first concerns the microwave characterisation, modeling and design services, the second one is dedicated to the manufacturing of microwave products including characterization setups, and the last one concerns the Research and Development of innovative microwave products and new characterization benches.

Main Tasks within E^{2}COGaN:

- WP3: Development of pulsed measurement set-ups (600V->1000V, 10A, ns-pulses) and DC and pulsed HV characterization including specific probes to perform tests on wafer and characterization procedures on wafer for this high voltage devices; contribution to reliability assessments including HTRB, self-heating, trapping,

Profile and Expertise:

MC2 technologies is located in North of France, 12 employees are working on electrical characterization and modeling of active devices. The idea is to establish the links between the electrical performances and the devices design. For all that, several innovative setups and characterization procedures have been developed in order to be able to determine the potentialities of the devices. These setups are available in our catalogue. To illustrate these setups we can propose an automatic and multiharmonic active load pull setup based on a PNAX platform, an accurate and fast noise measurement setup working in the frequency bandwidth 4-40GHz and also a high voltage pulsed IV system working up to 600V. MC2 technologies has been or is involved in European Projects (FP7, ENIAC, etc.), such as EFFISEC and PANAMA but also in National contracts such as ANR MEMSGAN

CV of Staff scientists involved:

Dr. Nicolas Vellas (MC2 technologies CEO): received his PhD. degree in Electronic, with Honour, from University of Lille 1, France. He carried out this thesis in the frame work of the common laboratory named "TIGER" between the "Institut d'Electronique, de Microelectronique et de Nanotechnologie" and "Thales-TRT" on microwave characterization in small and large regime of gallium nitride transistors for very high power applications. During this thesis, He has authored or co-authored more than 30 papers in international conferences and journals and three patents concerning the development of innovative microwave tuners and of a very high sensitive near and far field correlation radiometer. In parallel of the thesis, he worked on the MC2-Technologies company creation.

Dr. Christophe Gaquière: received the Ph.D. degree in electronic from the University of Lille in 1995. He is currently professor at the University of Lille, and carries out his research activity at the Institut d'Electronique de Microélectronique et de Nanotechnology (IEMN).
The topics concern design, fabrication and characterization of HEMT's and HBT devices. He

works on GaAs, InP, metamorphic HEMT's and now he is involved in the GaN activities. His main activities are microwave characterizations (small and large signal between 1 and 500 GHz) in order to correlate the microwave performances with the technological and topology parameters. Today, his activities concern mainly the investigation of two-dimensional electronic plasmons for THz solid state GaN based detectors and emitters, AlGaN/GaN nano-wires for microwave applications and high voltage DC/DC convertors. He is directly related to the MC2 technologies activities as CTO and co-founder of this company.

(13) CONSORZIO NAZIONALE INTERUNIVERSITARIO PER LA NANOELETTRONICA (IUNET)

Description of the Legal Entity:

The "Consorzio Nazionale Interuniversitario per la Nanoelettronica" (IUNET, Italian Universities Nano- Electronics Team), is a non-profit, private Organization, which has been created with the initial aim to lead and coordinate the effort of the major Italian University Teams in the field of Silicon and Compound Based Nanoelectronic Device Modeling and Characterization. After this initial phase, several other groups have joined IUNET, bringing competences in analog, mixed-mode and digital IC design, electronic systems, algorithms for signal processing and power devices based on III-V and III-N semiconductors.

Current Members of IUNET are the Universities of Bologna, Calabria, Ferrara, Modena e Reggio Emilia, Padova, Pisa, Roma "Sapienza", Udine, and the Politecnico of Milano. They offer renown and complementary expertise in the field of modeling, simulation, design, characterization of CMOS-based nanometer-size electronic devices as well as in the development of algorithms and architectures for signal and information processing and power generation.

Main Tasks within E^{2}COGaN:

- WP3: Work package Leader, reliability, robustness and safe operation area assessment of GaN power devices including photospectroscopy, DLTS, trap modeling, 2D/3D simulation of devices...
- WP6: Strong commitment to dissemination

Profile and Expertise:

IUNET is a world-wide known leader in the assessment, understanding and modeling of complex device reliability and instability phenomena in GaN power devices.

The Microelectronics Lab of the Information Engineering Department of the University of Padova is active in the field of microelectronics circuit and devices design, characterization and reliability since 20 years. Among the various topics of research, the Microelectronics Lab is recognized worldwide as a leading group in the field of reliability physics, and has achieved important results advancing the understanding of the reliability of CMOS integrated circuits, MEMS compound semiconductor devices, GaN High Electron Mobility Transistors, GaN-based Light Emitting Diodes and lasers, and, more recently, organic semiconductor transistors, solar cells and OLEDs.

CV of Staff scientists involved:

Prof. Gaudenzi Meneghesso is a Full Professor of Electronics at the University of Padova and will act as WP3 leader. He graduated in Electronics Engineering at the University of Padova in 1992 working on the failure mechanism induced by hot-electrons in MESFETs and HEMTs and received the Italian Telecom award for his thesis work. In 1997 he received the Ph.D. degree in Electrical and Telecommunication Engineering from the

University of Padova working on hot-electron characterization, effects and reliability of GaAs-based and InP-based HEMT's and pseudomorphic HEMT's. His research interests are: i) Electrical characterization, modeling and reliability of power, microwave and optoelectronic devices on compound semiconductors; ii) Electrical characterization, modeling and reliability of RF-MEMS switches for reconfigurable antenna switches; iii) Study of the sensitivity of Electronics devices to Electrostatic discharge and development of suitable protection structures; and iv) Characterization and reliability of organic semiconductors devices. Within these activities he published about 500 technical papers (of which more than 50 Invited Papers and 6 best paper awards). He has been the General Chair of three conferences: HETECH 2001, HETECH 2008, WOCSDICE 2007 and ESREF 2012; He has been the Technical program Chair of WOCSDICE 2001, of the International Electrostatic Discharge Workshop (IEW) 2010 and he has been the TPC co-chair of ESREF 2010. He is in the steering committee of several European conferences. He also served several years for the IEEE-International Electron Device Meeting (IEDM) and He is serving in the Management committee of IEEE International Reliability Symposium (IRPS). He is Associate Editor of the IEEE Electron Device Letter for the compound semiconductor devices area since 2007.

Prof. Enrico Sangiorgi is a Full Professor of Electronics at the University of Bologna. From 2005 to 2010 he is the Director of IUNET. Since 1994 he is Editor of IEEE Electron Device Letters. He has been a member of the following Conference Technical Committees: IEDM (’91-96; ’04-’06), ESSDERC (‘99-present), INFOS (’95-‘03), ULIS (’00-‘07), etc. Enrico Sangiorgi coauthored 33 papers presented at the IEDM, and overall more than 160 papers on journals and conference proceedings. He is a Fellow of the IEEE and he has been involved in managing European Projects of the 5th, 6th, and 7th FP. Since 2007 he is a member of the Strategic Board of the AENEAS Association.

(14) Universität Kassel, Kompetenzzentrum für Dezentrale Elektrische Energieversorgungstechnik (KDEE)

Description of the Legal Entity:

The KDEE (Centre of Competence for Distributed Electric Power Technology) was founded in January 2009 as a separate structural unit within the University of Kassel. It was in part originated from the Power Electronics group from the ISET e.V (Institute for Solar Energy Technology), which had a long term expertise in the design and construction of power converter for photovoltaic systems. Since its founding, the KDEE works in close cooperation with the Department of Electrical Power Engineering (EVS), where Prof. Zacharias is the head. The KDEE/EVS has currently a pool of more than 20 engineers, working within several industry cooperations (SMA Solar Technologies, VW AG, Hadler, EON-Mitte, Infineon Technologies, etc.) and state-funded projects.

Main Tasks within E^{2}COGaN:

- WP1: Provision of demonstrator specifications and translation into functional requirement specifications
- WP5: Conception, implementation and evaluation of PV string-inverter demonstrator

Profile and Expertise:

Main activities are directed towards the development of power electronics systems especially designed for renewable energy sources like Photovoltaic and Wind; along with decentralized and mobile conversion systems for automotive systems. The design of highly efficient systems is supported by the investigation and application of new semiconductor technologies, including SiC and GaN, alongside the characterization and design of highly

efficient magnetic components. The group was among the first worldwide to built and test a photovoltaic inverter with SiC devices, reaching the first efficiency record for such circuit. These and other activities take place in cooperation with several industry partners.

CV of Staff scientists involved:

Prof. Dr.-Ing. habil. Peter Zacharias received the Dipl.-Ing. and the Dr.-Ing. degrees in electrical engineering from the "Otto-von-Guericke" University Magdeburg, Germany, in 1979 and 1981, respectively. During 1983 and 1984 he was a postdoctoral researcher at the Polytechnical Institute of Kiev in power laser engineering. He worked at the University of Magdeburg until 1990 as associate professor for power electronics with the research fields of power electronics for high voltage applications and pulsed power. From 1990 to 1995 he worked at Lambda Physik GmbH Goettingen responsible for power systems development for excimer lasers. 1995 he joined the Institute for Solar Energy Technology (ISET) Kassel, Germany, and headed the power electronics department until 2001. In 2001 he changed to eupec GmbH in Warstein, Germany, as manager for power assemblies. In 2005 he joined the University of Kassel as professor for Electric Power Supply Systems and founded in 2009 the Centre of Competence for Distributed Electric Power Technology (KDEE).

M.Sc. Samuel Vasconcelos Araujo received the Bachelor's degree in electrical engineering from the Federal University of Ceará, Brazil, in 2006, and the Master's degree in science in renewable energies and energy efficiency (RE2) from the University of Kassel, Kassel, Germany, in 2007, where he is currently finishing the Ph.D. degree. He worked in the ISET e.V (now Fraunhofer IWES) for two years on the development of power electronic circuits in partnership with the industry, testing the very first photovoltaic inverters operating with SiC devices. He is currently with the Centre of Competence for Distributed Electric Power Technology (KDEE), University of Kassel, and is coordinating several projects in the field of power electronics and new semiconductor technologies. His research interests include the design and optimization of power circuits and the investigation of innovative semiconductors based on wide band-gap materials. He will act as WP5 leader.

(15) COMMISARIAT A L'ENERGIE ATOMIQUE ET AUX ENERGIES ALTERNATIVES (CEA-LETI)

Description of the Legal Entity:

LETI is the Laboratory of Electronics and Information Technology of CEA – the French Atomic Energy Commission. LETI was created in 1967 in Grenoble and is one of the leading research institutes in Europe Its mission is to develop innovative solutions which leads to industrial transfers or start-up creation and, meanwhile to explore prospective fields in collaboration with academia. LETI's activities cover Silicon technology, micro system technology, optical components, multimedia, transmission and telecommunication systems, design, and micro technologies for health and biology. The driving programs of LETI are linked with Minatec – the innovation centre in micro- and nano- technologies - and with Nanotec300 - the 300mm infrastructure to take up the challenge of micro- and nano-electronics. In 2011, Leti's staff is now around 1100 people and about other 500 people coming from industrial partners and academic research institutions is also working on the site. The budget is around 250 MEuros, including about 200 MEuros of external resources, with about 50M€ capital expenditure.

Main Tasks within E^{2}COGaN:

- WP2: Conception, design, process development, implementation and characterization of GaN power devices (including 8" device demonstrators)

Profile and Expertise:

CEA-LETI is currently running CMOS processes on 200mm and 300mm wafers in two adjoining areas of its clean room facilities of more than 3000m2. In particular, the 200mm area is currently equipped with epitaxial tool for GaN power device development. Both areas are used for the work with industrial partners and wafers are regularly exchanged with industrial facilities as all protocols for contamination control and traceability are in place. The processing capabilities are supported by over 80 advanced characterization tools of which a number are on-line in the clean room and capable of handling both 200mm and 300mm wafers

CV of Staff scientists involved:

Dr. René Escoffier studied Electronic Engineering at University of Montpellier II. He was granted his PhD in 1995 on the numerical simulation of the trapping-de-charge trapping in oxides subjected to ionizing radiation. He has developed TCAD software for ISE (Zurich) and then joined Motorola in 1999 to design protections structures against ESD (Electro Static Discharges). He then worked for Onsemiconductor and Freescale where he developed power MOSFETs for automotive. He joined power team of CEA-LETI Grenoble in 2010. He is currently working at CEA-LETI on the power components (wide gap) and their integration into modules for electric vehicle applications. (rene.escoffier@cea.fr).

(16) FRAUNHOFER-GESELLSCHAFT ZUR FOERDERUNG DER ANGEWANDTEN FORSCHUNG E.V (FhG)

Description of the Legal Entity:

Research of practical utility lies at the heart of all activities pursued by the Fraunhofer-Gesellschaft. Founded in 1949, the research organization undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration.

Main Tasks within E^{2}COGaN:

- WP2: Monitoring of the impact of structural epitaxy defects (dislocations, etc.) on device performance and stability (IISB)
- WP4: Work package leader (IZM), Assembly (IZM) and gate driver activities (IMS) including high temperature solutions

Profile and Expertise:

IZM: Fraunhofer IZM is a centre for highly robust technologies used for system integration. A main part of the past work has been focused on power electronic packaging. The project will broaden the range of knowledge to integration of GaN devices and integrating them to complete systems with enhanced operating temperatures. The gained knowledge on technologies, reliability and models will put the institute in the position to adapt project results to a range of other application conditions. This will be offered as an R&D services following the general terms of the Fraunhofer Society.

IMS: Fraunhofer IMS runs its own 200mm CMOS Fab with a 250C high Temperature SOI process including W metallisation and has a strong focus in the high temperature electronics field. Currently customers in this field mainly come from low volume and high price markets like oil and gas drilling industry. The results of this project will enable IMS to enter the field of

power electronics and energy saving with this high temperature electronics.

IISB: Fraunhofer IISB conducts applied research and development in the fields of micro- and nanoelectronics, power electronics, and mechatronics. IISB has more than 10 years of experience in material development and characterization of GaN. By the project, IISB will transfer its knowledge on reliability issues of power devices from Si and SiC to GaN.

CV of Staff scientists involved:

Dr. Stefan Dreiner (IMS) is head of the group "semiconductor processes and devices" at Fraunhofer IMS. He has many years of experience in technology and device development, TCAD simulation, device characterisation and parameter extraction (bulk and SOI processes).

Holger Kappert (IMS) is group manager of the high temperature electronics group at Fraunhofer IMS. He has more than 15 years of experience in mixed-signal CMOS circuitry and embedded system design. He was responsible for a large number of publicly funded and industrial projects regarding all kinds of R&D activities in the field of circuit design.

Dr. Hermann Oppermann (IZM) is heading the group Interconnect Metallurgy & Processes. He is an experienced project manager in interdisciplinary projects related to the integration of power and high temperature electronics, MEMS, Solid State Lighting and photonics, and System-in-Package (SiP) development. His main research interest is metallurgy and reliability related to interconnects.

Dr. Olaf Wittler (IZM) is heading the department Environmental and Reliability Engineering and will be the WP4 leader. Since 1999 he is working in the field of mechanical and thermal reliability of electronics and electronic packages where he was responsible for a range of public and industry funded R&D projects with a focus on thermal and reliability characterization and modeling.

Dr. Jochen Friedrich (IISB) is head of the IISB crystal growth department since 2004 and is leading the Fraunhofer Techology Center for Semiconductor Materials (Freiberg) in cooperation with ISE since 2005. Emphasis of his R&D is on PV silicon, bulk growth and epitaxy of wide bandgap semiconductors, detector and laser materials.

Dr. Patrick Berwian (IISB) is group manager of epitaxy and layer deposition with a focus on wide bandgap semiconductors, yield, reliability and quality control issues.

(17) Slovak University of Technology in Bratislava (STUBA)

Description of the Legal Entity:

The **Slovak University of Technology in Bratislava (STUBA)** is attended by almost 18000 students and belongs to leading universities in microelectronics education and R&D activities in the New Member States of EU. The Institute of Electronics and Photonics of STUBA is active in a field of microelectronics, photonics and sensorics. Its membership in EUROPRACTICE provides access to advanced TCAD modeling and simulation as well as IC design tools (Synopsys, Cadence, H-Spice). Structure and device characterization and failure analysis either by electrical (I-V, C-V, DLTS measurements in a wide temperature range with optional magnetic field, microwave characterization) or analytical and optical tools (SEM, EBIC, CL, AES, AFM, SIMS, micro-Raman spectroscopy) is another strong field of institute activities. The comparison and good correlation of experimental and simulated results is used for physical models calibration, physical interpretation of obtained experimental results and prediction of the properties of new semiconductor devices and IC's. The actual activities comprise thin film sensors and subsequent signal processing for

healthcare and environmental applications, analogue and mixed signal design, smart power MOS device design and characterization, GaN based devices, organic semiconductor transistors and LED's, diamond and carbon nanotubes growth. The well equipped laboratories, expertise and enthusiasms of department staff ensure the successful project solution. They are about 50 teachers and researchers and 30 PhD students at the institute. They actively participated in projects in 5th, 6th and 7th FP projects as well as NATO and COST projects. More than 20 projects funded by national authorities and/or within bilateral international collaboration are being solved at the institute yearly.

Main Tasks within E^{2}COGaN:

- WP2: Device Simulation (TCAD) and Device Characterization
- WP3: Complex Device Characterization supported by 2/3-D modeling and simulation, extraction of compact "Spice like" transistors models

Profile and Expertise:

Complex structure and device characterization and failure analysis either by electrical (I-V, C-V, DLTS measurements in a wide temperature range with optional magnetic field, microwave characterization) or analytical and optical tools (SEM, EBIC, CL, AES, AFM, SIMS, micro-Raman spectroscopy) is a strong field of institute activities. They are supported by 2/3-D TCAD modelling and simulation. Thin film sensors and subsequent signal processing for healthcare and environmental applications, analogue and mixed signal design, smart power MOS device design and characterization, GaN based devices, organic semiconductor transistors and LED's, diamond and carbon nanotubes electronics are another competencies of institute.

CV of Staff scientists involved:

Prof. Jaroslav Kováč graduated at the Slovak University of Technology (STU), Faculty of Electrical Engineering and Information Technology (FEI STU), Bratislava, in 1970. Since 1971 he has been engaged in the research of optoelectronic devices technology at the Microelectronics Department of FEI STU. In 1983 he received a PhD degree and in 2001 professor degree at STU Bratislava. Since 1991 he has been the team leader of the Optoelectronic and Microwave group at the Department of Microelectronics. His interests and expertise include technology and advanced characterisation of optical and electrical properties of III-V devices by electrical, optical and analytical methods. He was involved in many framework research projects and act as a national coordinator of 5 FP project VGF GaP and 7 FP project MORGaN. The results of his work were published in more than 300 papers in scientific journals and international conference proceedings.

Prof. Alexander Satka received the MSc. and PhD degrees in Electronics, both from Slovak University of Technology (STU) in Bratislava, Slovakia, in 1984, and 1995, respectively. From 1995 to 1999 he was Researcher at Microelectronics Department, FEI STU in Bratislava. Since 2005 he has been Associate Professor and 2011 Full Professor in electronics at the same department. He was involved in several basic and application oriented research projects. Currently, he is involved in the research programs of two FP7 projects, 3 Slovak research and 2 application-oriented projects. He is also a coordinator of the research grant funded by the Slovak Ministry of Education, and key project personnel in one FP7 project (SMASH, FP7-NMP-2008-LARGE-2). His research activities are oriented mainly to diagnostics and characterization methods of semiconductor and optoelectronic structures and devices. The results of his scientific work were published in more than 250 papers in peer reviewed journals and international conference proceedings.

Prof. Daniel Donoval is a full professor and director of Institute of Electronics and

Photonics. He is involved particularly in physics, technology and characterization of advanced semiconductor structures and devices supported by TCAD modeling and simulation. He has been a referee of the projects submitted within FP of European Union. Currently he is a member of the Education & Training Coordination Board and management team of the Scientific Community Council of ENIAC. He is the Slovak representative in Public Authorities Board and governing Board of ENIAC JU. He coordinated many R&D projects supported by national and international agencies. He authored and co-authored more than 230 papers published in international scientific journals and conference proceedings. To stimulate the technology transfer to industrial partners he organizes many conferences, workshops and participates in scientific program and steering committees of many international conferences.

(18) University of Bristol (UNIVBRIS)

The University of Bristol is one of the leading universities in the UK. 31 of the University's departments achieved the top grades of 5*/5 in the UK research assessment exercise (RAE), including the H.H. Wills Physics Laboratory and its Center for Device Thermography and Reliability (CDTR), leading the University of Bristol's contribution to this project. The University of Bristol is ranked as top-100 university in the recent OS World University Ranking 2012. Its prime target areas are research and higher education.

Main Tasks within E^{2}COGaN:

- WP3: Characterization, understanding and modelling of thermal properties on device level.
- WP4: Characterization, understanding and modelling of thermal properties on advanced discrete and module solutions.
- WP6: Work package Leader, active contribution to dissemination activities.

Profile and Expertise:

The Center for Device Thermography and Reliability (CDTR), H.H. Wills Physics Laboratory, headed by Professor Kuball and its members (senior member: Prof Uren (Research Professor), Dr. Sarua (Senior Research Fellow), five postdoctoral researchers and five PhD students), has internationally leading expertise and capabilities in the thermal, electrical and reliability study of advanced electronic devices, experimental and simulation, in particular of wide band gap semiconductor materials and devices such as based on GaN or diamond. In this project the CDTR will use its extensive thermal analysis and simulation expertise.

CV of Staff scientists involved:

Prof. Martin Kuball, director of the CDTR in Bristol (since 1997), is internationally leading expert in the thermal study as well as reliability study of semiconductor devices, in particular, of wide band gap electronic devices (GaN and others). As principle investigator, he is presently leading several UK, European and US programmes funded by the UK research council EPSRC and TSB, as well as Ministry of Defense (MoD), EC-FP 7 (AGAPAC), ONR Global (DRIFT), DARPA (NJTT), European Space Agency ESA (GREAT^2), European Defence Agency EDA (MANGA), and various contracts with UK, European and US companies (e.g. TriQuint USA, Group4Labs USA, Northup Grumman USA, UMS Germany, Thales Alenia Spaciale France, Selex UK). Professor Kuball has management expertise in leading various large scale technology development programmes. He has more 200 publications in semiconductor research, has given 30 invited presentations and tutorials on wide bandgap electronics in the recent five years. He has organized various national and international conferences, and is member of programme committees in the field of wide

bandgap electronics. Prof. Kuball obtained his PhD from the Max-Planck Institute for Solid State Physics, Stuttgart and the University of Stuttgart, Germany, in 1995.

Dr. James W. Pomeroy, lead postdoctoral researcher in the CDTR, obtained his PhD from the University of Bristol in 2006, and since then has co-supervised three PhD students in the CDTR. Dr Pomeroy has key expertise in the thermal analysis and thermal simulation of GaN devices, and corresponding technique developments, with more than 30 publications in this research field, and has recently given an invited presentation on thermal characterization of GaN electronics at the MRS Fall Meeting 2011 in Boston, USA. Dr. Pomeroy obtained his PhD degree from the University of Bristol in 2006.

(19) Synopsys Switzerland LLC (SNPS)

Description of the Legal Entity:

Synopsys Schweiz LLC is a leading provider of Technology CAD (TCAD) solutions for the Semiconductor Industry. The company was founded in 1993 as Integrated Systems Engineering AG (ISE AG) as a spin-off from ETH Zurich and was acquired by Synopsys Inc., in November 2004. SNPS currently employs about 50 people in Zurich, most of them highly specialized scientists working as software developers or application engineers. Its main customers are R&D and design for manufacturing departments of leading semiconductor manufacturers world-wide. Synopsys TCAD offers a comprehensive suite of products that includes the industry leading process and device simulation tools, as well as a powerful GUI-driven simulation environment for managing simulation tasks and analyzing simulation results. The Synopsys TCAD process and device simulation tools support a broad range of applications such as CMOS, power, memory, optoelectronics, analog/RF and laser. In addition, Synopsys TCAD provides tools for interconnect modelling and extraction, providing critical parasitic information for optimizing chip performance. With the multidimensional device simulator Sentaurus Device, SNPS offers a modern simulator which gives the user the flexibility of implementing device simulation and circuit models via a physical model interface (PMI).

Main Tasks within E^{2}COGaN:

- WP3: TCAD application as well as model development and calibration for simulation of GaN power devices with the focus on trapping/de-trapping mechanisms, hot carrier effects, thermal effects, and radiation influence.

Profile and Expertise:

SNPS has developed a group focusing on TCAD model calibration and model development over the last 10 years. SNPS within its device simulator already developed the III-V models for drift-diffusions and hydrodynamic simulations. SNPS provides the compute environment to run large DOE's necessary for model calibration and device optimizations. SNPS has built over the last years expertise in GaN RF power devices modelling and thermal modelling through projects like THERMINATOR and with leading customers worldwide.

SNPS has a vital interest in keeping its simulators up-to-date with all necessary models for the simulation of current and future technologies. Therefore, the development activities are strongly influenced by customer demands and are performed in close collaboration with the leading research institutes. Synopsys Switzerland LLC (former ISE AG) has successfully participated in the semiconductor related ESPRIT projects PROMPT, PROMPT II, SUBSAFE, in the IST FP 6 projects MAGIC-FEAT, MULSIC, DEMAND, FRENDTECH, SINANO, and ATOMICS, and in the FP 7 projects NANOSIL, THERMINATOR, and ATEMOX as well as in a number of other EU projects. SNPS is also involved in the ENIAC

project MODERN.

CV of Staff scientists involved:

Dr. Ronald Gull, Director TCAD C&E, graduated in electrical engineering from ETHZ in 1992 and received his Ph.D. from the Swiss Federal Institute of Technology Zurich in 1996 titled "TCAD Based Development of a Polysilicon Emitter Transistor in a BiCMOS Technology. Joined Integrated System Engineering AG specialized in semiconductor process and device simulation as an application engineer and promoted to leading Support and Pre-Sales with responsibility at the executive management level. In 2005 he joined Synopsys Switzerland as director of the worldwide TCAD Consulting and Services group.

Dr. Axel Erlebach, Principal, graduated in theoretical physics at the University of Technology in Dresden (TUD) in 1987. He joined the semiconductor company "Centre of Microelectronics" in Dresden in 1987. From 1991 until 1997 he was with the Fraunhofer Institute IMS in Dresden and received his PhD in physics in 1998 from the University of Duisburg in Germany. Since 1997 he is with Synopsys Switzerland LLC (until 2004 ISE AG). He is author and co-author of about 45 technical and scientific publications, filed several patents in the field of semiconductor sensors and Microsystems and has 22 years experience in the field of modelling and simulation of semiconductor processes and technologies.

(20) Bitron Spa (BIT)

Description of the Legal Entity:

Founded in 1955, Bitron designs, manufactures and markets of a broad range of electronic and mechatronic devices and systems. The worldwide customer-base includes major manufacturers of cars, motorcycles, household appliances and energy systems. The quality management system is certified to ISO 9001 and ISO/TS 16949 and the environmental management system to ISO 14001. Recognitions include prizes from Toyota and Yamaha for project management, logistics and quality.

Main Tasks within E^{2}COGaN:

- WP1: components/modules specification
- WP2: Technology monitoring
- WP5: DC/DC board-net converter demonstrator design and prototyping

Profile and Expertise:

Bitron has R&D, manufacturing and sales and marketing facilities throughout the world and regularly participates in international, multi-disciplinary projects. The electronics division is situated in Grugliasco (Turin), Italy, where R&D and one of the main manufacturing units are situated. Providing cost-effective, energy-efficient hardware and software solutions, Bitron has developed custom and general purpose static converters and motor controls, with several tens of thousands of units sold. Together with the CNR in Pisa, Bitron is a founder member of SPIN Italia (Software Process Improvement Network), part of the Software Engineering Institute, a consortium aimed at embedded software quality improvement. Software/firmware development capabilities are SPICE certified (Software Process Improvement Capability dEtermination).

The close interaction between HW and SW design, procurement, quality assurance and

process engineering will ensure that performance, economic, quality and reliability objectives are kept in focus throughout the project.

Bitron is leader in the FP7 collaborative project AVTR and partner in the FCH-JU project D-CODE in the ENIAC-JU project IDEAS.

CV of Staff scientists involved:

Giuseppe Catona graduated in Electronics Engineering at the Politecnico of Torino in 1996, with a thesis on design and prototyping of a 3kW electronic arc welder. He worked at Fiat Research Centre from July 1997 to March 2011, mainly involved in electronic HW design for automotive systems. In particular he has developed both DC/DC converters and three-phase inverters for hybrid vehicle. More recently he gave the main contribution to the conception and realization of the high performance power converters and digital controls for the Formula1 Kinetic Energy Recovery System (KERS) also heading the Automotive Power Electronics Group. In April 2011 He joined BITRON, where we is now responsible for the activities on motor drives and power converters for electric traction and stationary applications.

Dr. Marco Ottella received his degree in Electronic Engineering in 1996 and his Ph.D in Electrical Engineering in 2001, at the Politecnico of Torino. He has been working at CRF since 1996 where in late 2007 he joined the Hardware Design and Development Department participating in numerous projects on the design of power electronics for hybrid and electrical powertrain (Kinetic Energy Recovery Systems, Fiat 500 Hybrid,…) and promoting the public funded initiatives on the electrification. In this position, as a member of the coordination group, he promoted, wrote and managed the major projects on fully electrical vehicles in the JU ENIAC and ARTEMIS and in the PPP CGI (E3CAR, POLLUX, IoE, MotorBrain, IDEAS, CASTOR, PMOB, WIDE-MOB, HI-WI, SmartLic,…). In early 2012 he left CRF to promote and coordinate the public funding initiatives inside the BITRON Group. He is co-author of a consistent number of patents and international papers on electrical drives.

Enrico Bianconi holds a degree in Electronic Engineering from the University of Pisa. Prior to joining Bitron, he held positions in the R&D organisations of Magnetek (now Power-One), Magneti Marelli and International Rectifier. He has 15 years of experience in power electronics and energy systems and holds several patents.

Annamaria Ceccia got the electronic engineering specialist degree course at University of Salerno in 2010. She currently works in the research and development energy conversion systems department in Bitron SpA Grugliasco Italy since February 2011.

She is involved in power converters for electric vehicles and before she has designed circuits for photovoltaic applications.

(21) Schneider Electric (SE)

Description of the Legal Entity:

Schneider Electric is a global specialist in energy management with operations in more than 100 countries; Schneider Electric offers integrated solutions to make energy safe, reliable, efficient, productive and green across multiple market segments. The Group has leadership positions in energy and infrastructure, industrial processes, building automation, and data centres/networks, as well as a broad presence in residential applications. In 2011 , Schneider Electric has $22,4bn Global Sales with 39% of sales in new economies The group has more than 130 000 employees.

Schneider Electric is offers products and solutions for 5 main markets:

(1) Energy & Infrastructure (main customers: Electrical utilities, water & waste treatment plants, Public sector investors, oil & gas infrastructure, Marine sector, etc.)

(2) Industry (main customers: Engineering firms, systems integrators, OEMs, large industrial companies, panel builders and electrical equipment distributors, end users.

(3) Data centers and networks (main customers: From small companies to global groups, hospitals, administrations, etc. Our customers are where the availability and quality of the electrical energy is critical.)

(4) Buildings: (main customers: Developers, engineering offices, developers, engineering and design firms, systems integrators, contractors, panel builders, electrical equipment distributors, building operators and end users.

(5) Residential: (main customers: Architects, building owners, developers, building contractors, electricians, electrical equipment distributors, DIY superstores and end users.

For all these markets, our products and services solutions cover: Processes control and supervision, Power supply & distribution, Energy monitoring and control, Utility management (lighting, ventilation, elevators, intruder alert, etc, Smart electrical networks management, Single site or multi-site production data management, Critical power, Machine control and monitoring, Architecture design and installation audits,Leading-edge UPS systems, electrical switchgear, generators, etc, Cooling systems with a unique rackbased cooling technique to avoid overheating.

Innovation and R&D

Schneider electric invests between 4 to 5% of its sales in R&D activities with more than 8600 engineering in 25 countries. The main R&D hubs are based in Grenoble, Shangai, Bangalore and Boston. The main objective is to develop solutions that not only optimise efficiency and reduce costs, but also deliver increased simplicity, ease of use, and environmental benefit. These new responses to the issues of energy efficiency and the emerging Smart Grid incorporate high technology products, services, and software.

Main Tasks within E^{2}COGaN:

- WP1: Work package Leader & specification of GaN power devices for industrial power inverters application & demonstrator
- WP5: GaN-based converters: development of power converter for test of GaN power devices and evaluation of the gain brought by these devices at system level for industrial applications as motor drive, UPS or solar Inverter.

Profile and Expertise:

Schneider Electric's Innovation department focuses on research & advanced development on cross-businesses topics:

- Solution frameworks,
- Platforms and components,
- Base technologies,
- Processes and supporting tools

Innovation is a about 200 people global organization with presence in France, US, China and India working in 4 main teams:

- Energy efficiency,
- Software
- Innovation efficiency
- Technology Innovation

The Technology Innovation team within Innovation is working on Leverage leading edge technologies to accelerate product and solution innovation in support of Schneider Electric's strategy, with specific focus on electro-mechanics, power electronics, embedded software and communication. Since several years the team based in Grenoble is working on topics as

Electric Vehicle charging, Microsolar plants, Smart Grids and new WBG devices as SiC and GaN. The team has very large experience on the use of these devices in power inverters.

CV of Staff scientists involved:

Dr. Radoslava Mitova graduated from the French department of Electrical Engineering (Technical University of Sofia) in 2001. She received Ph.D degree in Integration in Power electronics from the National Polytechnic Institute of Grenoble in 2005. She also worked for a in Primes Lab (Tarbes, France) on high voltage architectures with medium voltage transformer for railway traction. She joined Schneider Electric in 2007 and she is involved in industrial anticipation projects in power electronics and in particular on new material power semiconductors (SiC, GaN). She has experience in several FP6 &FP7 European (MinAmi, SmartPower) and national joint projects (HOMES, SiCHT2) coordination and WP leadership.

(22) Azzurro (AZZURRO)

Description of the Legal Entity:

The AZZURRO Semiconductors AG had been founded as start-up by 2003 out of the University Magedeburg, with headquarter in Germany. AZZURRO is technology leader in the epitaxy of GaN on Si-substrates. In 2005, first crack free 150mm GaN-on-Si wafer were demonstrated. In 2010, start of mass production of GaN-on-Si wafer with closing round C financing of 14.5Mio. Euro. In 2011, move to the new production facility in Dresden with epitaxy on new multi-wafer MOVPE-reactors and completing the management team with around 45 employees in 2012. The company offers worldwide commercially available HEMT-, LED- and Template-Epitaxy-wafer with 2“, 100mm and 150mm wafer diameter [http://www.azzurro-semiconductors.com/]. AZZURRO provides high performance GaN-on-Si based HEMT- and LED-wafer as innovation in PowerElectronics- and LED-applications like power conversion and lighting.

Main Tasks within E^{2}COGaN:

- WP2: Research for epitaxy of 150mm and 200mm HEMT-epi-wafers for 800V and new buffer concepts for device epitaxy up to 1500V, including simulations, optimization and characterization of GaN power devices (Schottky diodes and HEMTs)

Profile and Expertise:

AZZURRO brings in R&D entity located at Dresden, with about 9 employees for R&D activities. Its expertise lies in the epitaxial growth of GaN-based HEMT epitaxy on Si-substrates, design simulations and characterization with a strong focus on HV devices. AZZURRO is involved in two German funded Projects (Neuland, GaNonSi).

CV of Staff scientists involved:

Dr. Stephan Lutgen is Vice President at AZZURRO Semiconductors AG in Magdeburg/Dresden in Germany. He received his diploma in physics 1993 at the Phillips University of Marburg. After his PhD on III-V semiconductors - obtained in 1997 at the Humboldt University in Berlin - he joined Siemens in Regensburg. He worked 3 years as MOVPE-engineer in production of GaAs based LEDs and laser. In 2000 he joined the R&D team of GaAs-based laser at Osram OS as project leader for laser development of frequency doubled IR-laser for blue and green semiconductor laser in highly innovative ultra-compact rgb-laser projection technologies. In 2005 he started as project leader for direct blue GaN based laser diodes and was leading the Osram-activities in different BMBF-projects for visible laser. In 2008 he was heading the R&D-

department for direct blue and green GaN-based laser diodes at Osram OS in Regensburg. In 2010, he and his R&D-Team were awarded with the Karl-Heintz-Beckurtspreis for their pioneering work on GaN-based direct green laser diodes. After successful R&D work on green laser and blue power laser diodes in small TO packages he joined the AZZURRO Semiconductors AG in 2011 as Vice President Technology.

(23) Robert BOSCH GmbH (BOSCH)

Description of the Legal Entity:

The Bosch Group is a leading global supplier of technology and services. In the areas of automotive and industrial technology, consumer goods, and building technology, some 285,000 associates generated sales of 47.3 billion euros in fiscal 2010.

Bosch considers occupational training an integral part of its social responsibility. Worldwide more than 6,600 young people, of whom around 4,600 are in Germany, receive high-quality training of this kind.

In the field of research and development with some 34,000 associates, Bosch's expenditure totals 3.8 billion euros (8,1 % of sales). In 2010 we applied for over 3,800 patents worldwide.

At Bosch, the way we do business is in tune with environmental protection. Already back in 1973, the Bosch Group specified protection of the environment as being one of its business objectives – it is therefore assigned the same high importance as the quality of Bosch products and the efficiency with which the company does business. Bosch is determined to enhance the quality of life of people all around the world with solutions that are both innovative and beneficial.

Bosch is celebrating its 125th anniversary in 2011. The company was set up in Stuttgart in 1886 by Robert Bosch (1861–1942) as "Workshop for Precision Mechanics and Electrical Engineering." The special ownership structure of Robert Bosch GmbH guarantees the entrepreneurial freedom of the Bosch Group, making it possible for the company to plan over the long term and to undertake significant up-front investments in the safeguarding of its future. Ninety-two percent of the share capital of Robert Bosch GmbH is held by Robert Bosch Stiftung GmbH, a charitable foundation. The majority of voting rights are held by Robert Bosch Industrietreuhand KG, an industrial trust.

Main Tasks within E^{2}COGaN:

- WP1: Requirements on power electronics coming from automotive needs and requirements from interconnection technologies on chip-back-end processes
- WP4: Assembly and interconnection technologies for high temperature and highly robust GaN power module concepts
- WP5: Assembly support for demonstrator build up

Profile and Expertise:

The Corporate Sector Research and Advanced Engineering (CR) is responsible for the development of new technologies and product innovation in areas such as automotive electronics, car multimedia, energy and body systems, safety and security systems, software engineering , digital signal processing algorithms, very large scale integration, and manufacturing techniques. The mission of CR is to look ahead 5 years and more in technology landscape. More than 1.000 employees are working for a sustainable technology future in industrial services, e. g. as automotive tier 1 supplier or photovoltaic cells manufacturer. The department CR/APJ has a lot of experiences on electronics joining and assembly technologies more over than two decades. Over 20 scientist experts are working on future pcb assembly processes and power module technologies. Life-time determination

by reliability testing and attending simulations completes the profile of the department.

CV of Staff scientists involved:

Dr. Martin Rittner is senior expert for assembly and interconnection technologies in power electronics in the CR of Bosch. He received his diploma in Nuclear Physics 1994 at the University of Stuttgart and finished his PhD thesis 2001 in Semiconductor Physics at 4th Physical Institute. Since then he attended several national and EU public funded projects over the last ten years in the field of electronics packaging for Bosch CR. For the national automotive supplier industry he is currently managing the ZVEI working group 'High temperature and Power Electronics'.

(24) Technical University of Eindhoven (TU/e)

Description of the Legal Entity:

The TU/e concentrates its distinctive disciplinary research strengths in strategic areas around a limited number of major societal issues. The first two TU/e Strategic Areas relate to the themes of Energy and Health while a third Strategic Area around the theme of Smart Mobility is being considered in respect of desirability and feasibility. The Strategic Areas serve as an interface between chairs and sub-departments within the university, on the one hand, and with non-governmental bodies, companies and other knowledge institutions on the other. In the case of the latter, external parties, TU/e develops and shares knowledge for application within society. These Strategic Areas provide the framework for the development of roadmaps and consortia with other universities, knowledge institutions and companies. This gives that the TU/e has a real focus, mass and quality within relevant research domains as well as a stronger social profile for the university, more revenue capacity in secondary and tertiary funding plus greater attractiveness to potential students. The research cooperation between TU/e and industry and other knowledge institutions will be considerably strengthened by the Strategic Areas. Furthermore, TU/e encourages specific research institutes and research-driven, high-tech companies to locate at the university campus.

Main Tasks within E^{2}COGaN:

WP5: Modeling and simulation tools for GaN-based SCCs in combination with piezo-electric transformers in a distributed matrix structure; Exploration of GaN-based topologies and circuits that are optimal with respect to size, efficiency, and ripple performance.

Profile and Expertise:

Eindhoven University of Technology (TUE) Electromechanics and Power Electronics (EPE) group has an extensive expertise in the fascinating field of advanced methods and tools to enhance the analysis, design and multi-objective optimization of innovative electromagnetic structures and cyclically switched networks. The TUE EPE group conducts high-level fundamental research in the societal and market needs area of Electromechanics and Power Electronics, with emphasis on modeling, analysis, design methodologies and multi-objective optimization of mechatronic and energy conversion systems. Theoretical research is therefore combined with ultra-fast numerical tools and supported by dedicated experiments. The group is collaborating in many national and international projects and has many connections with leading industries. The TUE EPE group has expertise in multiple national and international R&D projects. Moreover, lately it is noticeable that challenging electrical system and power electronics applications experience a large attraction on trainees, graduate and postgraduate students. State-of-the-art laboratories for testing and characterization (1000m2) are available in the EPE group.

CV of Staff scientists involved:

Prof. dr. E.A. Lomonova was born in Moscow, Russia. She received the M.Sc. (cum laude), Ph.D. (cum laude) degrees and scientific title of Ass. Prof. (Docent - awarded by the Russian Ministry of Higher Education) in Electromechanical Engineering, all from the Moscow State Aviation Institute (TU), Russia in 1982, 1993 and 1998, respectively. Currently she is a full-time professor and chair of the group of Electromechanics and Power Electronics (EPE) at Eindhoven University of Technology, The Netherlands. She is a member of the Executive Council of the European Association of Power Electronics.

Ir. M.A.M. Hendrix received the MSc. degree in electronic circuit design from the Eindhoven University of Technology (TU/e), The Netherlands, in 1981. He is currently a Senior Electronics Architect at Philips Innovation Services, Eindhoven. In 1983 he joined Philips Lighting, Eindhoven, where he started to work in the Pre-Development Laboratory, Business Group Lighting Electronics and Gear (BGLE&G). Since that time he has been involved in the design and specification of switched power supplies for solar inverters, low and high pressure gas-discharge lamps, and LEDs. In July 1998, he was appointed a part-time Professor (UHD) with the Electromechanics and Power Electronics (EPE) group, TU/e, where he teaches a design-oriented course in power electronics below 4 kW.

Dr. J.L. Duarte received the MSc. degree in 1980 from the University of Rio de Janeiro (COPPE), Brazil, and the Dr.-Ing. degree in 1985 from the INPL Nancy, France. He has been with the TU Eindhoven, EPE group, as a member of the academic staff, since 1990. His teaching and research interests include modeling, simulation and design optimization of power electronic systems. In 1989 he was appointed a research engineer at Philips Lighting Central Development Laboratory, and since October 2000 he has been consultant engineer on a regular basis at high tech industries around Eindhoven.

(25) AUDI AG (AUDI)

Description of the Legal Entity:

Audi is one of the world's leading automotive premium brands, and builds high-quality, technologically progressive cars that are among the most admired on the international market. An advanced, forward looking approach to corporate management and development constitutes the basis of our success. We place our customers' wishes at the very heart of our unceasing quest to find ever better solutions. This philosophy is reflected in our brand claim "Vorsprung durch Technik".

Main Tasks within E^{2}COGaN:

- WP 1: Specification and requirements to ensure applicability for mass production
- WP 5: Reviews to incorporate lessons learned; design validation and product verification; performance bench test on electric vehicle

Profile and Expertise:

Audi also develops advanced hybrid and electric car – branded etron. These developments are supported by experts and specialists who also review all electronics being developed at/for Audi. This comprehensive support enables a fast comprehensive lessons learned between project. Robustness and quality for Audi starts at the component level. The existing level of competence from component specification and validation to a complex system level is the foundation of high quality system for our customers. Involving these experts also

ensures the know-how transfer inside Audi into various other projects.

CV of Staff scientists involved:

Berthold Hellenthal holds a degree (Dipl-Ing.) in mechanical engineering from the RWTH Aachen in 1993; experience in: (a) semiconductors, (b) design of AC/AC converters from 3kW to 20kW, (c) automotive hardware development. Current position: fellow on automotive hardware in the mechatronic competence center supporting electronic developments at Audi. Mr. Hellenthal is also responsible for the Audi semiconductor strategy, the Audi Progressive Semiconductor Program (PSCP).

8.3 Consortium as a whole

8.3.1 Overview

As the highest goal of the E^{2}COGaN project is to demonstrate GaN power devices as a disruptive power device technology on application level, one of the key strategies behind the set-up of the consortium was to map the entire GaN power electronics value chain from substrate provider (AZZURRO, EPIGAN), to semiconductor manufacturer (ONsemi, NXP, and ST-I), to module makers (Semikron), Application Providers (BOSCH, CIRTEM, BIT) and finally system manufacturers (AUDI, EADS and SE) as illustrated in Figure 19. In addition, hard- and software and service providers were added such as MC2, Synopsis, NANO and CISC to add further expertise and competences in device and system simulation or in measurement set-ups and characterization methodology. Also for the academic partners and research institutes, we cover the total range from substrate engineering and characterization (CEA LETI, FHG-IISB), device engineering and characterization (CEA LETI, IUNET, UNIVBRIS, STUBA), advanced module and assembly techniques and their characterization (FHG-IZM), advanced gate driver concepts (FHG-IMS, CEA LETI) and finally application experts such as TU/e and KDEE. Moreover, the partners are chosen in such a way that we can assess the GaN potential in relevant applications for several key markets such as Automotive (AUDI, BIT, CIRTEM), photovoltaic (KDEE, ST-I) with pre-studies in industrial (SE) and aeronautics (EADS).

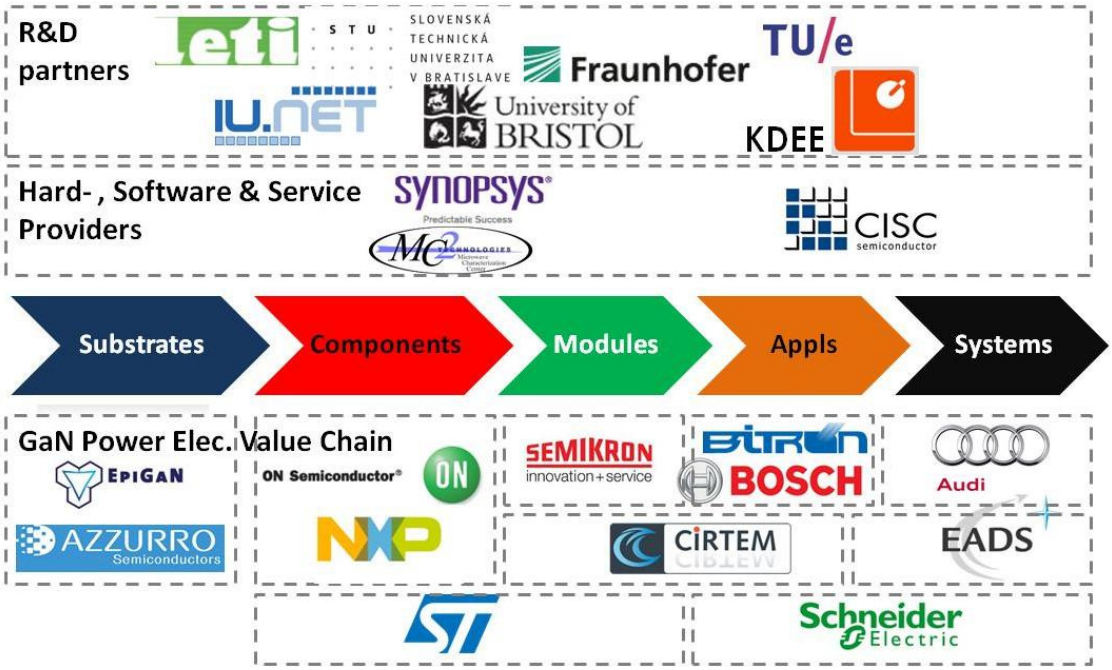

Figure 19: Positioning of the E²COGaN industrial and R&D partners with respect to the GaN power electronics value chain: a complete mapping of the value chain is obtained both by the core industrial partners, the hard-, software and service providers and the R&D institutes.

Furthermore, special attention has been paid to the choice of the right partner and the right number of partners for optimal risk mitigation. All partners are recognized in their fields and have ample experience in European Projects such as ENIAC or FP7. The number of partner has been chosen to have for all potential bottlenecks in the value chain at least two partners, such as for substrates, devices and modules. GaN is not yet a mature power device technology and important risks are present along the whole project work flow. Especially, the impact of GaN on assembly, module, gate driver choices has hardly been studied yet. Moreover, different applications are likely to require different epitaxy, device and module implementations, which cannot be assured by one single substrate or one single device provider alone. The chosen set-up therefore guarantees that the project's targets will be met with a high probability.

Last, but not least, the E²COGaN project unites 25 partners, which are well shared over a total of 9 European Countries (AT, BE, CH, DE, FR, IT, NL, SK, UK) in their work contribution (cf. Figure 20). Among the partners E²COGaN has a total of 6 SMEs coming from 5 different European countries that have an essential commitment in the project. Their contribution (in terms of person-months) amounts to 18% of the project, compared to 54% for large industrial partners and 28% for academics and institutes (cf. Figure 21). The large industrial partners will be in the driving seat, but both academics and SMEs will benefit through the close collaboration required to reach the project goal. Of the total eligible cost about 2% is dedicated to subcontracting.

As a summary, E²COGaN comprises a consortium which is at the level of its ambitions. Covering the full value chain and 9 European states, it will lay down the seeds for a future European GaN power electronics ecosystem with sustainable growth and high level jobs.

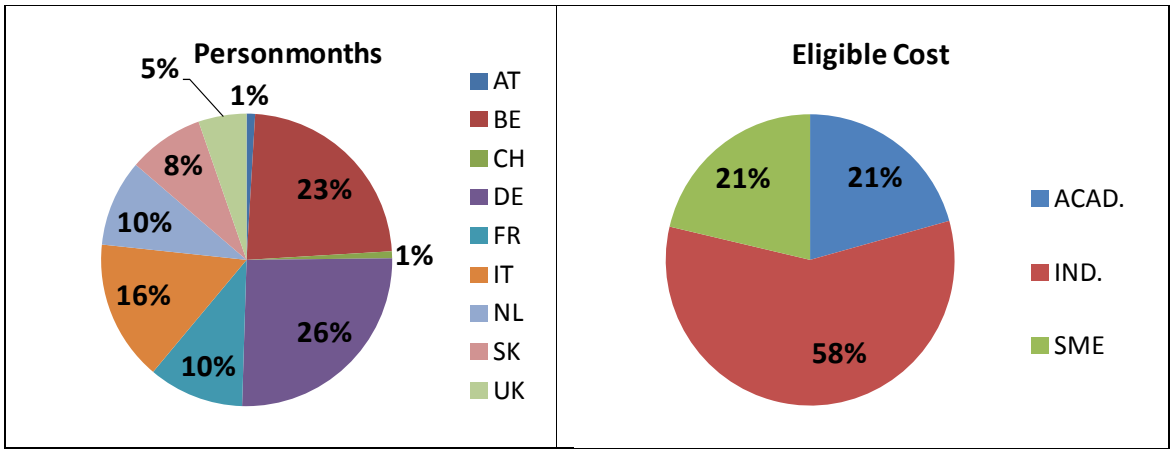

*Figure 20: Break-down of the person*months and eligible cost over the 9 participating European countries.*

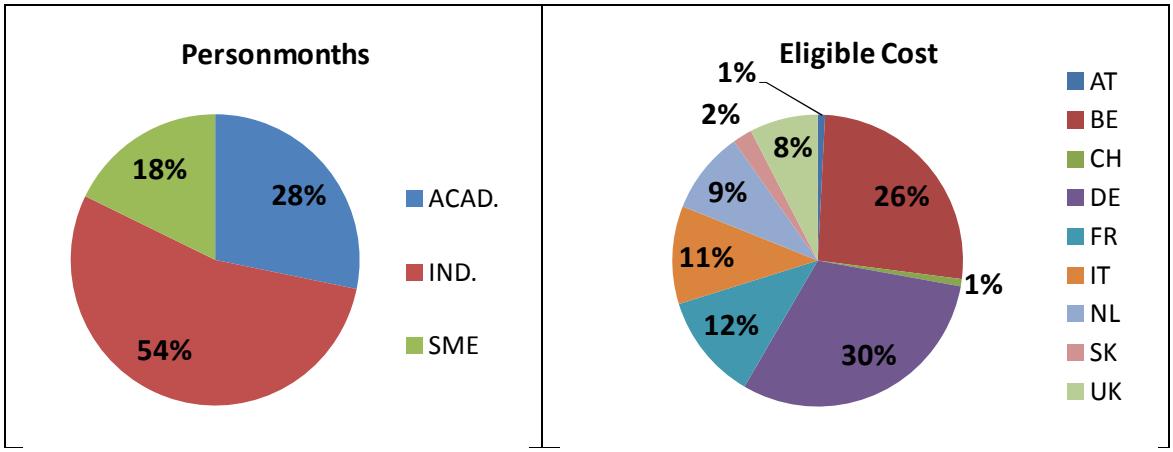

*Figure 21: Break-down of the person*months and eligible cost over the type of institution.*

8.3.2 Third parties:

The "Consorzio Nazionale Interuniversitario per la Nanoelettronica" (IUNET, Italian Universities Nano-Electronics Team) is a non-profit, private organization, aimed at leading and coordinating the efforts of the major Italian university teams in the field of silicon-based nano-electronic device modelling and characterization. Current members of IUNET are the Universities of Bologna, Calabria, Ferrara, Modena e Reggio Emilia, Padova, Pisa, Roma "Sapienza", Udine and the Politecnico di Milano. As such it qualifies as "Grouping" under the definition given in Article II.14.2.B of the "Guide to Financial Issues relating to FP7 Indirect Actions", and therefore as third party carrying out part of work and entitled to funding, since it can be considered among: "associations, federations, or other legal entities composed of members (in this case, the Grouping is the beneficiary and the members contributing to the project should be listed)."

The partners of IUNET involved in E^{2}COGaN are the following:

- Università di Bologna
- Università della Calabria
- Università di Modena e Reggio Emilia
- Università di Padova.

The specific competences and expertise brought to the project are related to i) the understanding of parasitic phenomena in GaN-based Power devices, through: advanced characterization and device modeling and assessment of technological countermeasures, ii) of 2D / 3D device simulations of GaN-based devices with special focus on parasitic phenomena and breakdown behavior; iii) Identification of device failure modes and mechanisms and recommendations towards the development of a robust and reliable GaN–based technology. This contribution is relevant to the project and is testified by the very large number of relevant papers published in international journals, the long-standing collaboration with leading industries in the field and the extremely significant recognition at international level of all the involved team members, as it can be deduced by their CVs.

Allocation of Person-months among the IUNET partners:

IUNET	**WP1**	**WP2**	**WP3**	**WP4**	**WP5**	**WP6**	**WP7**	**TOTAL**
Università di Padova			**33.5**			**0.5**	**1**	**35**
Università di Bologna			**22.5**			**0.5**		**23**
Università di Modena e RE			**19.5**			**0.5**		**20**
Università della Calabria			**11.5**			**0.5**		**12**
TOTAL - IUNET			**87**			**2**	**1**	**90**

8.4 Small and Medium size Enterprises

The E^{2}COGaN project counts a total of six SME's, i.e. 25% of the consortium, located in 5 different European countries (Austria, Belgium, France, Germany, Slovakia) which are integrated into the heart of the project. All of them have large responsibilities and are therefore key for the success of this project.

Azzurro (spin-off of the University of Magdeburg) and EpiGaN (spin-off of IMEC) are the project's main GaN epitaxy substrate suppliers. They are heavily involved in WP2 and constitute the first level of the GaN power electronics value chain as mapped out in the E^{2}COGaN project. CIRTEM, specialist in advanced power converters, represents the other end of the value chain being fully responsible for one of the project's major demonstrators, the EV battery charger. CISC is providing service to power device and power electronics manufacturers via sophisticated simulation software and libraries and will take the opportunity to adapt the simulation tools to GaN devices. MC2 Technologies develops and provides very advanced pulsed IV measurement set-ups allowing the analysis of ns switching up to 600V (commercially available) or even 1000V (under development and part of E^{2}COGaN) combined with the characterization competences and skills as needed for the exploration of very fast switching in GaN devices within WP3. Last, but not least NanoDesign Ltd. as a spin-off of the University of Bratislava provides services to the industry in the measurements of semiconductor devices and will be one of the essential partners in the reliability assessment of WP3.

After having explained how the six SMEs contribute to the project's success the following paragraphs summarize how the project will be beneficial for the business development of the individual SMEs.

AZZURRO Semiconductors AG is a small size Enterprise and technology leader on the epitaxy of GaN on Si-Substrates. The company provides worldwide HEMT-, LED- and

Template-Epitaxy-wafer with diameter of 2“, 100mm and 150mm for commercial applications (http://www.azzurro-semiconductors.com/). With the development of future 200mm epi-technology-platform for HEMTs with higher breakdown voltage and new e-mode devices (150mm and 200mm) Azzurro will address the high power electronic market in the framework of this project. Epi-Design, 2D-HEMT-simulation and epi-wafers from AZZURRO will be done in close cooperation with the project partners for wafer processing, device testing with focus on HV applications.

Power electronics is facing a technological breakthrough induced by the rising maturity of the game-changing "wide gap" components. As a center of innovation in this area, **CIRTEM** is committed to offer high power density converters in the medium term. This requires access to components or chips of new technology tailored to our design. Only via collaborative projects such as E^2COGaN early access to these new power devices can be established enabling further internal evaluation and use in applications. The realization of technological demonstrators is a prerequisite for access to new markets, however the underlying necessary developments are expensive and risky. In this respect, the E^2COGaN offers an excellent opportunity for the development and validation of these demonstrators and therefore ultimately to address new markets.

EpiGaN N.V has been created in 2010 as a spin-off of imec. While its new production facility has been inaugurated in May 2012, EpiGaN is today starting production from its new site in Hasselt and is therefore actively hiring and expanding. Participation in this project is of higher importance for this young company as it will allow EpiGaN to work closely with the large device companies active in the field, and to whom they may be potential supplier. Deep understanding of the product specifications on one hand, and possibility to perform R&D to meet those specifications on the other hand are key interests for this SME to join the consortium. This project will enable EpiGaN also to expand its current product offering by moving to higher voltage ranges and lower channel resistivity than currently available. This is expected to allow EpiGaN to remain at the leading edge of high quality GaN-on-Si epiwafers for electronics.

About 30% of **CISC**’s turnover is related to the existing simulation framework product System Architect Designer (SyAD®, www.cisc.at/SyAD) and the Modelling Library. As a common trend many OEM and tier 1 customers using this simulation framework shift their interest more and more in simulation from system exploration more towards system optimization. In this context the optimization potential of such a system is essential in the case of use of GaN technology. So far these models at that level do not exist or will be provided on a case by case basis.

The integration of CISC within the project will be linked with semiconductor manufacturers (as e.g. ST-I) and companies from the application domain (as e.g. BIT). CISC will explore to what extent the models need to be generated, what are the suitable modeling languages (and simulators) and how they can be derived effectively form a set of technology parameters that are released to public.

NanoDesign Ltd. is a spin-off company, focused on rapid technology transfer of expertise in precise measuring in field of bioelectronics and semiconductor testing. Strong connection to STUBA University promotes academia-industry partnerships and helps to improve the educational process of young researchers and PhD. students with their orientation to industrial practice with promising results. Achieved results in field of structure and device characterization and reliability testing stimulate the collaboration in own and common research projects. NanoDesign Ltd. participates besides other projects in the Technological Competence Centre of Bratislava as one of most progressive companies in terms of flexibility and research potential in microelectronics. Participation in this project provides NanoDesign with great chances to establish new international partnerships with high exploitation potential of achieved results in very promising field.

For **MC2 technologies** involvement in this consortium is a real opportunity for several reasons:

The opportunities to develop a pulsed IV setup (1200V 20A) which is not available on the market and which will be required to validate the potentialities of the WBG devices, validate the technology evolutions, analyze the traps and thermal limitation effects. This setup is also needed to develop the future applications in order to elaborate the electrical equivalent scheme in the real conditions. Furthermore, several WBG technologies will be available which will validate the pulsed IV equipment following the electrical conditions. Last, but not the least, all main European actors are involved in this consortium. Hence, MC2 will have the possibility to demonstrate the potentiality of their system to establish the electrical equivalent schemes for circuits design or to establish the link between the technological parameters and the electrical performances.

The second aspect for MC2 technologies will be to implement an electrical characterization procedure on wafer at high voltage condition thanks to specific probes. These ones will be developed within the company in the framework of this project. Thanks to that, all the influence of the packaging will be studied. Moreover, the technology quality can be validated on wafer for a production aspect this will be the trick point.

8.5 Resources to be committed

Breakdown of the E^{2}COGaN resources

Concerning the spread over the different work packages within the project, more than half of the resources (both in person-months and cost) is spent in work packages 2 (substrate and devices) and 3 (robustness and reliability). This is explained by two elements: first, by the above mentioned high cost of GaN epitaxy and substrates and thus also device development that will prevail for the near (but not medium!) future, and, second, by the critical role of these work packages: if these cannot fulfil the earlier set requirements in terms of device specifications and quality, the hereupon dependent goals of work packages 4 (Assembly and Gate Drivers) and 5 (Application Demonstrators) can hardly be reached threatening the major innovation objectives of the E^{2}COGaN project, i.e. the demonstration of the GaN power device technology in hand-selected, economically and society-relevant application demonstrators. Paralleling of GaN power device engineering and assessment via several partners is thus crucial for risk mitigation.

Beneficiary Number	Beneficiary Short Name	WP 1	WP2	WP3	WP4	WP5	WP6	WP7	Total Person months
1 Coordinator	ONsemi	7	231	61			1	12	312
2	NXP-NL	4	91	52	2	2	2	1	154
3	NXP-UK	4	61		2	4		1	72
4	NXP-B	4	55	10			2	1	72
5	ST-I	8	36	64	36	36			180
6	Semikron	1			72			1	74
7	CIRTEM	2.5			22.6	36.3	1		62.4
8	EPIGAN	1	50	2			2	1	56
9	CISC					16	2		18
10	NANO		2	36	30		1	1	70
11	EADS	2		20	22	8	2		54
12	MC2 TECHNOLOGIES			23			1		24
13	IUNET			87			2	1	90
14	KDEE	4			5.5	48	2.5		60
15	CEA LETI	1.5	43.5				1.5		46.5
16a	FHG IMS	1.8			55.6		2		59.4
16b	FHG IZM	2			91.14	2	2	1	98.14
16c	FHG IISB		41				2		43
17	STUBA		12	74			3	1	90
18	UNIVBRIS		0.5	23	2		2.5	1.3	29.3
19	SNPS		2.5	10	1		1	0.5	15
20	BIT	3	2			36			41
21	SE	6				7.5	0.5	0.5	14.5
22	AZZURRO		108						108
23	BOSCH	3			34	4		1.5	42.5
24	TU/e					27	1	1	29
25	AUDI	5				7			12

Table 5 Resource breakdown per partner and per work package

Subcontracting

As mentioned before, about 2% of the total budget amongst the partners in the consortium is used for subcontracting. The activities performed in subcontracting include:

For partner AUDI AG, its contribution in WP5 includes taking part in automotive short product validation of the automotive demonstrator including vibration & shock testing, temperature cycle testing (test planning, building of test & monitoring equipment, setting up tests, performing tests, evaluation of collected data, test reports). These tests and the final test in an electric vehicle are planned to be supported and executed externally under the guidance of Audi.

For partner Cirtem, the subcontracting efforts are related to the use of the PRIMES platform (Tarbes, France). The specific activities include the usage of clean room and associated equipment (oven, plasma cleaning, Xray, digidrop), as well as characterization tools for electrical,thermal and mechanical tests (dielectric, passive and active cycling, sheartest, sonoscan, etc.).

For partner Schneider Electric, specific activities for subcontracting are the design of PCB boards and the realization of the inverter demonstrator for testing of the GaN devices.

For partner MC2 Technologies, the planned subcontracting activities are related to the work performed in WP3 on characterization and reliability. In this context, MC2 Technologies will mainly develop new equipment which is not available on the market and which is mandatory to be able to determine the electrical wide band gap transistors performances for high energy efficiency converter. Following these measurements the transistors will be either modified regarding the technological aspects or modelled thanks to these measurements to design circuits and systems.

In order to develop a pulsed I(V) setup up to 1000V, 10A with short pulse width and short rise and fall times a lot of equipment like digital components, analogue components, boards hence specific devices are required. Therefore, MC2 Technologies plans to develop dedicated circuits, which will be developed in the clean room facilities of the Institute of Electronic Microelectronic and Nanotechnologies (IEMN). MC2 Technologies is a spin off of this institute and almost all the doctors involved in our company emanate from this institute. An agreement is signed between these two entities. This is one part of the subcontracting. Besides the development of these new equipments MC2 Technologies will subcontract the realization of mechanical parts seeing the high currents and voltages since specific elements are required and also the realization of specific boards for the FPGA circuits which will drives all the elements in the new equipment.

For the University of Kassel, a significant focus of the activities of the University of Kassel will be directed towards the operation of the GaN devices with very high levels of switching speed. This will be done in order to operate with the minimum amount of switching energy, thus enabling operation with higher frequencies and consequently smaller filter elements. A direct consequence of the operation at higher speeds is the higher level of oscillations and also conducted and radiated emissions of the circuit. In order to properly qualify the developed demonstrators for the single phase photovoltaic inverter (not only concerning the circuit but also indirectly the power module), standardized measurements need to be performed. The subcontracting activities cover the necessary measurements (at least two interactions for each PV demonstrator) covering the EN-61000-3 and EN-61000-4 series in both conducted and radiation spectra by an accredited laboratory from the Fraunhofer Institute IWES in Kassel.

For partner EADS, the main activities that are performed under subcontracting include radiation tests under neutron beam, design of electronic PCB's, and the management of PhD thesis.

For partner Fraunhofer IISB comprises of characterization with specialized high-end techniques at external facilities. The applied techniques will be X-ray synchrotron topography, and transmission electron imaging. Both types of characterization are crucial for an in-depth understanding of material and device defects.

Project Responsibilities versus resources

During the set-up of the E^2COGaN consortium and the definition of the individual partners' responsibilities with respect to the project goals, special attention has been paid in order to match these in the best possible way to the partners' staff capacity (inside and outside E^2COGaN), infrastructure (i.e. cleanrooms, tools, characterization facilities) and expertise and competences. The larger the partners' resources pool is the better the project will be able to cope even with unforeseen issues during execution as external resources can be mobilized for a finite time to overcome these obstacles.

The following table provides an overview over these items for each partner.

Partner	Resources to be committed		
	Personnel	**Infrastructure / Tools**	**Expertise**
1. ONsemi	Pool of 8 (senior) scientists working on GaN development program. 1 program coordinator and 1 financial controller for all project management and financial related activities.	6" GaN-on-Si fabrication facility for the fabrication of GaN power devices. Assembly in an engineering packaging line. Characterization and engineering testing in a technology characterization lab, reliability lab and failure analysis lab. Various measurement equipment dedicated for the testing of GaN power devices.	High voltage discrete device development and manufacturing. R&D in novel device concepts and technologies. Design, implementation and characterization of these technologies. GaN-on-Si process and device development. HV measurement and characterization, including measurement methodology development.
1. NXP-B	1 project coordinator, pool of 5 (senior) scientists working on GaN embedded in a larger Process Technology Device Team	HV, HC on-wafer, discrete measurement facilities (1100V, 3A) w/ high temperature stage TCAD and Cadence licences	Device Layout and design Characterization and HV Device physics HV Device simulation Process Technology
2. NXP-NL	Pool of 8 (senior) scientists working on GaN embedded in a larger Process Technology and Design R&D Teams	HV, HC on-wafer, discrete measurement facilities (1100V, 3A) w/ high temperature stage pulsed measurements (100ns) oscilloscopes TCAD and Cadence licenses Access to several cleanrooms, physical (TEM, SEM, etc.) and further electrical characterization facilities	Device characterization and device physics Device Layout and design HV Device and application simulation and modeling Application design and assessment GaN Process Development
3. NXP-UK	Pool of 4 engineers and scientists working on GaN process development, product development of GaN devices and applications support to develop technology demonstrators	6" Si fab for GaN power device processing Characterization lab Cadence TCAD	HV device process development and manufacturing GaN Process Development HV Characterization and qualification Application interface
4. NXP-B	Pool of 5 (senior) scientists working on GaN embedded in a larger Process Technology Device Team,	HV, HC on-wafer, discrete measurement facilities (1100V, 3A) w/ high temperature	Device Layout and design Characterization and HV Device physics

	coordination of WP2	stage TCAD and Cadence licences	HV Device simulation Process Technology
5. ST-I	Pool of 12 (senior) scientists on design, process, characterization, simulation and application embedded in larger Process Techno-logy and Design R&D Teams	6" and 8" Si fab for GaN power device processing Characterization lab Reliability lab Application lab Cadence TCAD	Device Layout and design Power device process development and manu-facturing GaN Process Development Power and analog Characterization and qualification Application interface Device simulation
6. Semikron	Pool of engineers of electri-cal engineering and mecha-tronics working on packa-ging, technology develop-ment circuit development and IC-design, device and system characterization	Package lines for different module assembly and techno-logies Hard- und software for module design, ther-mal and mechanical simulation, circuit simulation and IC-design Characterization and reliability lab	Package layout, simulation and assembly Circuit development, simulation and IC-design Device and system characterization and qualification
7. CIRTEM	1 senior scientist working on design of converters, packaging and project management, 1 junior scientist working on packaging, 2 seniors technicians working on electrical and mechanical design of converters	PRIMES platform (Tarbes, France) will be used to develop GaN power packaging. Facilities in Labège including simulations tools (pspice, matlab, psim), electrical and mechanical cad, measure and test tools with source and load for functional and EMC	Packaging layout and design. Driver, filter and control design of normally off and normally on wide gap power components Design, manufacturing and test of power converters from KW to MW.
8. EPIGAN	PhD scientists	MOCVD reactors, HR-XRD , contact-less Hall/sheet resistivity, wafer characterization tools	GaN epitaxial growth Material Characterisation
9. CISC	Pool of 2 senior design engineers plus 3 engineers working on ICT for simulation	Co-simulation platform for system evaluations applicable, e.g. for automotive applications with a set of library elements (in particular DC/AC /DC	System level simulation Modelling on device and system level Automotive power train application know-how (also from projects E^3CAR and

		converter)	POLLUX)
10. NANO	Pool of 10 scientists including PhD students	UIS measurement set-up (2000 V, 200 A), multipulse voltage stress, thermal chamber, low freq. noise measurement set-up, parametric analyzer, oscilloscope (20 GHz), TDR (20 ps),modular DSA oscilloscope,	Expertise in UIS test and robustness analysis, TDR analysis of input and outpu transistor (DUT) parameters, noise measurement, failure analysis
11. EADS	Pool of 5 research engineers working on power electronic, reliability and EMC characterization	HT characterization facilities, laser bench for radiation tests, EMC facilities.	Reliability of semicon-ductors (failure modes and mechanisms) Electromagnetic radiation effects on semiconductors Electromagnetic compatibility (EMC)
12. MC2	pool of 4 permanent staff members	HV, HC on-wafer, discrete measurement facilities (1100V, 3A) w/ high temperature stage, microwave characterization up to 110GHz Pulsed IV setup 600V 20A on fixture	Electrical characterization in DC and microwave in small and large signal Electrical device simula-tions in steady state and transient conditions
13. IUNET	pool of 10 permanent staff members pool of 10 doctorates and postdoctorates	well-equipped characterization lab including HV, HI, RF (20Ghz) DLTS set-up Emission microscopy Environmental chambers Synopsis Sentaurus 2D/3D Cadence	3D device simulation, advanced device charac-terization (up to 20 GHz), complementary techniques (PL, DLTS)
14. KDEE	pool of 5 permanent staff scientists, pool of 15 scientific assistants	AC/DC power supplies up to 2kV/80kW Active loads High precision power analyzer EMC Laboratory Automated switching cell for pulsed cha-racterization of power devices up to 1.5kV; 300A; T : -40-250°C	Power devices characterization (Si,SiC and GaN) and application Simulation, design and construction of power electronics circuits, including auxiliary supply, driving, control and power stage (passive and active elements) Photovoltaic power converter topologies and

		Licenses of software for circuit and device simulation (PLECS, Spice, Simplorer)	system approaches
15. CEA-LETI	Pool of 4 scientists working on GaN on 200mm pilot line. Pool of 3 researchers working on off line characterization platform.	200mm wafer pilot line: Epitaxy, Etching; Metallisation; Lithography… Characterization platform: XRD; HRXRD, PL, CL, AFM…	Device Layout and design GaN process developments Electrical and morphological Characterization. TCAD simulation
16a FhG IMS	Pool of 8 (senior) design engineers and scientists working on circuit design and technology development	Cadence design tools 200mm CMOS Fab, wafer level test equipment for electrical test and characterization	Mixed Signal CMOS Design, CMOS technology development high temp. electronics
16b FhG IZM	Pool of 9 (senior) scientists with expertise on modelling and test, thinfilm technology, assembly and encapsulation.	Wafer level packaging fab line for 4" up to 300 mm, labs for bonding & assembly, encapsulation, reliability qualification, analytics, electro-thermal and mechanical test and high end simulation capabilities	Thermal modelling and test, reliability modelling, mechanical test and materials models, development of packages, materials and processes, package related failure mode analysis.
16c FhG IISB	Pool of 7 (senior) scientists working on GaN embedded in a larger materials and device manufacturing and characterization team	Various defect characterization techniques (defect etching, high resolution CL and EDS, EBIC, direct access to SXRT and TEM) and electrical device testing	Technology optimization by correlation of structural properties (in buffer, epilayer and device) and electrical device properties (functionality, yield, reliability)
17. STUBA	Pool of 12-15 scientists (including 3-4 senior scientists and 8-10 PhD students and postdocs) involved in various characterization techniques and TCAD modelling and simulation	Synopsys TCAD tools, parametric analyzer, prober, DLTS, AFM, micro-Raman, SEM/EDS with 4 nanomanipulators, EBIC, spectra CL,	2/3-D TCAD modelling and simulation on Si and GaN, characterization of power devices, complex analytical, optical and electrical characterization of semiconductor devices, SPICE simulation
18. UNIVBRIS	1 permanent staff member, pool of 10 research fellows, postdoctoral researchers, research professors and doctoral researchers.	Raman, Raman-IR, time-resolved Raman thermography systems EL imaging and EL spectroscopy systems. Raman, photolumine-	Thermal and strain device characterization and related materials characterization (experiment & simulation) optical spectroscopy (PL, EL, Raman) and electrical

		scence spectroscopy systems Electrical device charact. equipment Thermal, thermo-mechanical and device simulation software.	characterization including reliability.
19. SNPS	Two senior scientists working on TCAD device simulation embedded in a large TCAD R&D and application team.	TCAD simulation software, large computer cluster	All kind of TCAD device and process simulation, calibration of TCAD tools, and software development
20. BIT	1 design engineer, 2 senior scientists and 1 production manager. External resources (subcontracting) for thermo-mechanical design and EMC simulation and/or characterization	Power supplies, active loads, licenses of software for circuit and device simulation	Simulation, design, prototyping and testing of power electronics circuits, including, control, driving and power stages (passive and active elements) Design and product validation for large-scale production
21. SE	pool of 4 power electronics engineers and technical staff	HV and HC Power devices test bench for dynamic characterisation (1500V, 200A) Well-equipped lab for electrical tests (oscilloscopes, high voltage & current generators…)	Dynamic device characterisation, Power inverter design and test
22. AZZURRO	Pool of 8 (senior) scientists in R&D-Team working on GaN on Si based HEMT-Epiwafer Development	Several multi-wafer MOVPE-Reactors and Epi-Analytics lab (XRD, Hall,..) for Epi-wafer characterisation, HV-wafer-prober for on-wafer mappings up to 2kV, 2D-device simulations based on TCAD-licence	Special know how in GaN-on-Si based buffer and HEMT Epi wafer growth technology and characterization, device physics, HV Epi-design and device modeling
23. BOSCH	1 main contact , pool of 5 (senior) scientists working on power module technologies in a larger process and reliability team	well-equipped assembly and inter-connection laboratory including soldering, sintering, bonding equipment and attending analytical equipment	Major process techno-logies characterization expertise reliability assessment
24. TU/e	pool of 4 senior staff members and 7 PhD students active in research	Well – equipped power electronics laboratory providing a research environment on the	Thermal measurement equipment: climate-temperature system (CTS) -40 ºC to +180 ºC,

	of power converters	design of power converters' topologies and their analog/digital control design.	chamber 1 m³, thermo CAM S40; wide band power analyzers development systems for digital Electronics PCB design systems, programmable logic-development systems
25. AUDI	pool of 4 hardware experts (senior to fellow); responsible developers of Audi onboard charger; responsible developers of hybrid and electric drive train	Validation equipment including: climate chambers, shaker for shock, and vibration testing, sensors and monitoring equipment, test bench for battery charging of automotive batteries	Hardware development (from the device to system level) Specifications and requirements of automotive ECU's (Electric Control Units) Robustness of automotive ECU's Development of ECU's for automotive mass production Design & product validation

Príloha 3

ku Zmluve o poskytnutí finančných prostriedkov na spolufinancovanie projektu výskumu a vývoja Spoločného európskeho technologického podniku ENIAC č. 324280/2012 (E2COGaN)

A. 1 Základné informácie o projekte		
Názov projektu	"Energeticky efektívne konvertory na báze GaN výkonových súčiastok", časť projektu: „Multipulzné testovanie spoľahlivosti výkonových prvkov pomocou UIS testovania pri vysokých teplotách"	
Akronym projektu	E2COGaN	
Odbor výskumu a vývoja[1]	20207 Mikroelektronika	
Charakter projektu	Aplikovaný výskum a vývoj	
Doba riešenia projektu	Od: 1. 4. 2013	Do: 31. 3. 2016
Celkové náklady na projekt (v eurách)	270 000	
Výška spolufinancovania projektu z prostriedkov MŠ VVaŠ SR (v eurách)	94 500	
Podiel spolufinancovania z prostriedkov MŠVVaŠ SR na celkových oprávnených nákladoch (v %)	35,0	
Zodpovedný riešiteľ projektu (meno, priezvisko, tituly, č. telefónu, e-mail)	Ing. Martin Daříček, PhD. 0903 744 442 martin.daricek@nanodesign.sk	

A. 2 Zodpovedná organizácia	**Základné údaje o zodpovednej organizácií**
Názov organizácie	NanoDesign, s.r.o.
Skrátený názov	NanoDesign
Adresa	Drotárska 19/a Bratislava, 811 04
Samosprávny kraj	Bratislavský
IČO	3674 4930
Príslušnosť k rezortu	Bez príslušnosti

[1] Podľa smernice č.27/2006-R z 21. decembra 2006 o sústave odborov vedy a techniky a číselníku odborov vedy a techniky

Typ organizácie	Spoločnosť s ručením obmedzeným
Odvetvie podľa OKEČ (odvetvová klasifikácia ekonomických činností)	71121
Štatutárny zástupca (meno, priezvisko, tituly)	Martin Daříček, Ing. PhD.

A. 3 Zoznam riešiteľov

Zoznam riešiteľov priamo sa podieľajúcich na riešení projektu

Meno a priezvisko	Tituly	Pracovné zaradenie	Dátum narodenia	IČO organizácie	Počet hodín	Podpis*
Martin Daříček	Ing. PhD.	Technický riaditeľ	19.09.1981	36744930	1500	
Martin Donoval	Ing. PhD.	Vedecký pracovník	19.05.1983	36744930	1500	
František Horínek	Ing.	Výskumný pracovník	13.11.1987	36744930	2500	
Ľubomír Sládek	Ing.	Výskumný pracovník	6.11.1985	36744930	3000	
Martin Jagelka	Ing.	Výskumný pracovník	30.8.1989	36744930	1500	
Peter Vančo	Bc.	Technický pracovník	5.9.1989	36744930	1000	

- Ja vyššie podpísaný v zmysle zákona č. 428/2002 Z. z. o ochrane osobných údajov, súhlasím so spracovaním osobných údajov Ministerstvom školstva, vedy, výskumu a športu SR počas doby archivácie údajov a to v rozsahu uvedenom v zmluve. Zároveň sa zaväzujem, že pri akejkoľvek zmene údajov uvedených v zmluve budem informovať Ministerstvo školstva, vedy, výskumu a športu SR o týchto zmenách a to v lehote do 30 dní. Osobné údaje môžu byť spracovávané a archivované najviac po dobu 10 rokov po skončení poskytovania prostriedkov štátneho rozpočtu Slovenskej republiky.

A.4 Zoznam riešiteľov

Ostatní riešitelia	Celkový počet ostatných osôb	1
	Súhrnná kapacita ostatných osôb v hodinách	1500
Spolu	Celkový počet zamestnancov	7
	Súhrnná kapacita zamestnancov v hodinách	12 500

B. Ciele, harmonogram a výstupy projektu

Anotácia projektu

Uvedený projekt je riešený v rámci európskeho technologického podniku ENIAC a správa sa podľa Nariadenia Rady (ES) č. 72/2008 z 20. Decembra 2008, ktorým sa zakladá spoločný podnik ENIAC a Štatútu spoločného podniku ENIAC, ktorý je prílohou tohto Nariadenia. STU Bratislava je spoluriešiteľom projektu, ktorého koordinátorom je ON Semiconductor Belgium.

Polovodičové výkonové zariadenia predstavujú základný stavebný blok konverzných obvodov a sú priamo spojené s bežnými životmi ľudí. Prevádzajú napätie z vysokého na nízke, využívané v bežnom živote. Význam a kľúčová úloha výkonových konverzných systémov sú obzvlášť dôležité v prípade, keď sú pripojené na batériu alebo limitovaný obnoviteľný zdroj energie, v ktorých predstavujú kľúčový prvok celkovej efektívnosti systému.

Výkonové spínače pre vysoké napätia sú vyrábané obvykle z kremíku. Napriek tomu kvôli intrinzickým vlastnostiam sa výhody technológie spomalili. Toto je hnacou silou pre výskum a vývoj v oblasti inovatívnych technológií, založených na materiáloch GaN a SiC. Cieľom projektu bude výskum, vývoj a príprava demonštrátora, založeného na technológii GaN-na-Si ako vysokonapäťovej technológie s vysokou elektrónovou mobilitou. Konzorcium je nastavené vhodne na poskytnutie adekvátneho prístupu od základného výskumu a výroby GaN výkonovej elektroniky až po osadenie do puzdra a následnú implementáciu v reálnej aplikácii.

Náplňou riešenia projektu E2COGaN je návrh, príprava a demonštrácia vlastností vysokonapäťových (vn) a vysokofrekvenčných (vf) výkonových prvkov (Schottkyho diód a tranzistorov s vysokou pohyblivosťou (HEMT) na báze heteroštruktúr GaN na Si, ako prelomovej technológie z priemyselného, spoločenského a environmentálneho hľadiska.

Kľúčové slová

UIS testovanie, výkonové polovodičové prvky na GaN, heteroštruktúry na báze GaN, HEMT tranzistory, vn a vf výkonové prvky, energeticky efektívne konvertory (meniče), fotovoltaika, autoelektronika

Ciele projektu

UIS (induktívne spínanie) testovanie je jedna z hlavných testovacích metód odolnosti výkonových zariadení. Problematika UIS testovania je veľmi aktuálna a dôležité v oblasti IO systémov najmä v automobilovom priemysle. V súčasnosti sú však UIS testovacie systémy konštruované na testovanie MOSFET a IGBT zariadenia. Pre účely realizácie overovania vlastností HEMT prvkov je potrebné realizovať modelové zmeny metódy testovania a navrhnúť a realizovať testovacie prvky. V súčasnosti sa prvky testujú pomocou niekoľkých pulzov. Príprava multipulzného testovacieho zariadenia s opakovanou záťažou a testovanie elektrických parametrov degradácie s overovaním dĺžky života výkonových prvkov.

Počas projektu bude realizovaná charakterizácia a analýza spínaných parametrov modulov D-/E-zariadení s rozlíšením pod 2 ns. Rozvoj nových metód charakterizácie, založených na spínacích vlastnostiach prvkov, rf charakterizácia testovacích prvkov, vytvorenie modelov HFET tranzistorov v závislosti od štruktúry a morfológie komponentov s dôrazom na spínacie vlastnosti, výstupnú kapacitu a odpor v zopnutom a vypnutom stave. Bude tiež riešená charakterizácia prechodového javu v rýchlych moduloch s rozlíšením pod 50 ps za pomoci metód časovej reflektometrie (TDR). Budú tiež realizované štandardné merania na čipe pri vysokých teplotách do 200 ºC s potenciálom testovania do 300 ºC. Zároveň budú navrhnuté metódy a na vysokoteplotné elektrické merania zapuzdrených zariadení (do 500 ºC) a následne bude skonštruované zariadenie na princípe uvedených metód využité pri multipulznom testovaní pri vysokých teplotách.

Súčasťou úloh projektu bude testovanie výkonových prvkov metódou UIS pri maximálnom napätí 2 kV a maximálnom prúde 100 A.

Harmonogram riešenia projektu		
Názov etapy	Začiatok	Koniec
Rozvoj metód merania UIS pomocou pripravovaného testovacieho zariadenia	04/2013	08/2014
Návrh testovacích sekvencií a overovanie technologických parametrov testovacieho systému	08/2013	05/2015
Rozvoj analytických metód charakterizácie spínaných parametrov D a E módu na čipe	02/2014	07/2015
Charakterizácia prechodových javov v rozdielne rýchlych prvkoch s cieľom využitia TDR metódy pre dosiahnutie rozlíšenia pod 50 ps	07/2014	11/2015
Návrh, príprava a realizácia tepelných meraní a meraní pomocou UIS testovacieho zariadenia, realizácia multipulzných meraní, optimalizácia automatického testovacieho systému pre testovanie pri zvýšených teplotách pomocou metódy UIS	02/2015	03/2016
Prezentácia dosiahnutých výsledkov, využitie a ochrana duševného vlastníctva	09/2015	03/2016

Očakávané výstupy riešenia							
Kategória	Výstupy	Rok 2013	Rok 2014	Rok 2015	Rok 2016		
Publikácie	Publikácie v recenzovaných vedeckých časopisoch a zborníkoch konferencií		1		1		
	Publikácie v nerecenzovaných časopisoch a zborníkoch konferencií			1			
Aplikačné výstupy	Model testovacieho zariadenia na multipulzný test UIS				1		
	Metóda analýzy výkonových prvkov pomocou			1			
Vzdelávanie	Počet diplomantov,						

a popularizácia vedy a techniky	ktorých práce súviseli s riešeným projektom		1		1		
	Počet doktorandov, ktorých práce súviseli s riešeným projektom	1	1	2	2		
	Popularizačné aktivity - prezentácia výsledkov na výstave (napr. týždeň slovenskej vedy)		1	1			
	Organizovanie vedeckých konferencií a seminárov		1		1		
Pridaná hodnota riešeného projektu výskumu a vývoja	Novovytvorené pracovné miesta (post-doktorandské miesta)	1			1		
	Vytvorené partnerstvo medzi akademickým a podnikateľským sektorom	1	1	1	1		
	Vyvolané projekty výskumu a vývoja		1		1		

Rozpočet projektu pre zodpovednú organizáciu (v eurách)					
Rok	2013	2014	2015	2016	Suma
Bežné priame náklady	21 200	24 800	24 800	4 800	75 600
Mzdové náklady	12 500	15 000	15 000	2 900	45 400
Zdravotné a sociálne poistenie	4 400	5 200	5 200	1 000	15 800
Cestovné výdavky	1 200	1 500	1 500	600	4 800
Materiál	1 600	1 500	1 500	100	4 700
Odpisy	0	0	0	0	0
Služby	1 500	1 600	1 600	200	4 900
Energie, vodné, stočné a komunikácie	0	0	0	0	0
Bežné nepriame náklady	5 300	6 200	6 200	1 200	18 900
Bežné náklady spolu	26 500	31 000	31 000	6 000	94 500
Kapitálové výdavky	0	0	0	0	0
Výška spolufinancovania projektu z prostriedkov MŠVVŠ SR (v eurách)	26 500	31 000	31 000	6 000	94 500
Výška vlastných prostriedkov žiadateľa	37 857	44 286	44 286	8 571	135 000

D.Čestné vyhlásenie štatutárneho zástupcu | Zodpovedná organizácia

Ja, dole podpísaný/á doc. Ing. Martin Daříček PhD., štatutárny zástupca záväzne vyhlasujem, že:

- Všetky údaje obsiahnuté v dokumentácii projektu sú pravdivé
- Projekt bude realizovaný v zmysle predloženého obsahu
- Zodpovedná organizácia súhlasí s pravidelnou finančnou kontrolou projektu
- Zodpovedná organizácia bude archivovať všetky účtovné dokumenty súvisiace s realizáciou projektu po dobu 5 rokov po skončení jeho financovania Ministerstvom školstva SR
- Dávam súhlas na výkon kontroly príslušným kontrolným orgánom MŠVVaŠ SR
- Zodpovedná organizácia bude dodržiavať legislatívu Európskej únie a platnú legislatívu SR

Som si vedomý možných následkov a sankcií, ktoré vyplývajú z uvedenia nepravdivých alebo neúplných údajov. Zaväzujem sa bezodkladne písomne informovať o všetkých zmenách, ktoré sa týkajú uvedených údajov a skutočností.

Podpis štatutárneho zástupcu žiadateľa a pečiatka

.....

Miesto.....

Dátum.....

Príloha 4

ku Zmluve o poskytnutí finančných prostriedkov na spolufinancovanie projektu výskumu a vývoja Spoločného európskeho technologického podniku ENIAC č. 324280/2012 (E2COGaN)

Tab.1 Rozpis celkových prostriedkov štátneho rozpočtu Slovenskej republiky na financovanie oprávnených nákladov projektu spoločného podniku v jednotlivých rokoch jeho riešenia (v eurách)

Deň/mesiac/rok	1 / 4 / 2013	2014	2015	31 / 3 / 2016
výška prostriedkov	26 500	31 000	31 000	6 000

Príloha 5

Predpokladaný rozpis celkových vlastných prostriedkov spolufinancovania NanoDesign, s.r.o. v projekte E2COGaN č. 324280/2012 spoločného podniku v jednotlivých rozpočtových rokoch jeho riešenia (v eurách).

Spolufinancovanie – predpokladaný rozpočet vlastných prostriedkov projektu firmy NanoDesign, s.r.o.					
Rok	2013	2014	2015	2016	Suma
Bežné priame náklady	30 286	35 429	35 429	6 856	108 000
Mzdové náklady	17 857	21 429	21 429	4 143	64 858
Zdravotné a sociálne poistenie	6 286	7 428	7 428	1 429	22 571
Cestovné výdavky	1 714	2 143	2 143	857	6 857
Materiál	2 286	2 143	2 143	142	6 714
Odpisy	0	0	0	0	0
Služby	2 143	2 286	2 286	285	7 000
Energie, vodné, stočné a komunikácie	0	0	0	0	0
Bežné nepriame náklady	7 572	8 857	8 857	1 714	27 000
Bežné výdavky spolu	37 858	44 286	44 286	8 570	135 000
Kapitálové výdavky	0	0	0	0	0
Výška spolufinancovania projektu z prostriedkov MŠVVaŠ SR (v EUR)	26 500	31 000	31 000	6 000	94 500
Výška vlastných prostriedkov žiadateľa	37 857	44 286	44 286	8 571	135 000

Podpis štatutárneho zástupcu príjemcu a pečiatka

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Miesto: Bratislava
Dátum: